Implementing and simulating low frequency inverters using high frequency transformers and devices

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IMPLEMENTING AND SIMULATING LOW FREQUENCY INVERTERS USING HIGH FREQUENCY TRANSFORMERS AND DEVICES

submitted by

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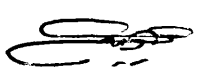

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Implementing and simulating low-frequency inverters using high-frequency transformers and devices

By

Mr. YEHIA ABOUFAKHER

Summary

This work makes a contribution to the study of the main and frequently used transformer-isolated converters and inverters. It starts by highlighting some of their major drawbacks and solutions are suggested to these drawbacks in order to improve power-converter performance. In particular the shortcoming of obtaining flux imbalance in push-pull dc/dc converters is investigated. High-frequency techniques were applied to transformer-isolated dc/ac inverters, and a review of low- and high-frequency transformation methods was performed. As a result of this survey, the best option, a low-frequency full-bridge dc/ac inverter, was designed and thoroughly investigated.

The effect of the main parasitic elements, such as stray and magnetizing inductance, equivalent series resistance in capacitors, ESR, on the performance of switch-mode power converters has been examined and to some extent taken into account.

In addition to examining transformer-isolated dc/dc and dc/ac converters practically, many component, circuit and system simulations have been performed and are used throughout this work to show typical waveforms and to verify the validity of methods of overcoming component, circuit and system problems. PSPICE simulation problems also had to be overcome, and methods for eliminating or reducing these problems have been examined. The MATLAB dynamic system simulator is suggested as an alternative to PSPICE in some situations where PSPICE is more difficult to use. The advantages of MATLAB compared to PSPICE are presented.

Particular attention has been paid to single- and three-phase transformer function and modeling both in PSPICE and MATLAB, and the simulation of transformer-isolated dc/dc converters in MATLAB has also been discussed. Finally, the operating changes in the junction and case temperature of power semiconductors have been modeled. This necessitated the precise modeling of the effects of MOSFET non-linear capacitances to accurately model switching loss effects, and the setting up of dynamic thermal models using power semiconductor device thermal-impedance curves.

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LIST OF SYMBOLS AND ABBREVIATIONS

Symbol	Definition	Unit
a.c.	Alternating voltage or current	[V or A]
A_e	Core effective cross-sectional area	[m^2]
A_n	Core factor	[$H/turn^2$]
B	Magnetic flux density ($=\phi/A_e$)	[T]
B_H	Highest flux density	[T]
B_L	Lowest flux density	[T]
B_r	Remanent flux density	[T]
B_S	Saturation flux density	[T]
B_W	Working flux density	[T]
C	Electrical capacitance	[F]
C_1	Core constant	[m^{-1}]
C_2	Core constant	[m^{-3}]
C_P	Specific heat	[cal/g°C]
C_θ	Thermal capacitance	[cal/°C]
d.c.	Direct voltage or current	[V or A]
DF	Dissipation factor	[F]
E	Energy	[J]
ESR	Equivalent series resistance of capacitors	[Ω]
f_O	Inverter output frequency	[Hz]
f_{SW}	Switching frequency	[Hz]
H	Magnetic field strength	[A/m]
H_C	Magnetic field strength coersivity	[A/m]
i	Instantaneous current	[A]
I, I_{AV}	d.c. or average current	[A]
I_C	Capacitor current	[A]

I_L	Load current	[A]
i_M	Magnetizing current	[A]
i_P	Transformer primary current	[A]
I_Q	Drain or collector current	[A]
i_S	Transformer secondary current	[A]
i'_S	Reflected secondary current in the primary	[A]
L	Magnetic inductance	[H]
l_e	Core effective magnetic length	[m]
L_L	Leakage inductance	[H]
L_{LKP}	Primary leakage inductance	[H]
L_{LKR}	Reset winding leakage inductance	[H]
L_{LKS}	Secondary leakage inductance	[H]
L_M	Magnetizing inductance	[H]
L_P	Primary inductance	[H]
L_S	Secondary inductance	[H]
L_{STRAY}	Stray inductance	[H]
M	Mass	[g]
MATLAB	MATrix LABoratory	
N	Transformer turns ratio	[-]
N_P	Number of transformer primary turns	[-]
N_R	Number of transformer reset winding turns	[-]
N_S	Number of transformer secondary turns	[-]
P	Power	[W]
P_e	Eddy-current loss	[W]
P_h	Hysteresis loss	[W]
P_{IN}	Input power	[W]
P_O	Output power	[W]
PSPICE	A commercial version of SPICE	
Q	Electrical charge	[C]
R	Electrical resistance	[Ω]
rms	Root-mean-square voltage or current	[V or A]

R_θ	Thermal resistance	[°C/W]
SPICE	Simulation Program with Integrated Circuit Emphasis	
t	Time	[s]
T_{OFF}	Turn-off time	[s]
T_{ON}	Turn-on time	[s]
T_R	Magnetizing-current reset-time	[s]
T_S	Period of switching cycle ($=1/f_{SW}$)	[s]
v	Instantaneous voltage	[V]
V, V_{AV}	d.c. or average voltage	[V]
V_a	Core actual volume	[m^3]
VA	Volt-Ampere product	[VA]
V_{CC}	Auxiliary supply voltage	[V]
V_{DC}	d.c. input voltage for a converter	[V]
V_{DO}	Threshold voltage of power diodes	[V]
V_{DS}	Drain-source voltage of a power MOSFET	
V_e	Core effective volume	[m^3]
V_{GS}	Gate-source voltage of a power MOSFET	
V_O	Output voltage	[V]
v_P	Transformer primary voltage	[V]
V_{QO}	On-state voltage drop of power switches	[V]
V_{REF}	Reference voltage	[V]
v_S	Transformer secondary voltage	[V]
Z_θ	Thermal impedance	[°C/W]
η	Efficiency	[-]
ϕ	Magnetic flux	[Wb]
ϕ_{MAX}	Maximum magnetic flux	[Wb]
μ_0	Absolute permeability ($= 4\pi 10^{-7}$)	[H/m]
μ_a	Amplitude permeability	[H/m]
μ_r	Relative permeability	[H/m]
θ	Phase angle	[rad/s]
τ	Time constant	[s]

CONTENTS

INTRODUCTION

In low power applications, relatively simple and easy-to-design linear power supplies are used, where a transformer followed by a rectifier, a regulator and a filter constitute the whole power supply. This configuration is shown in a block diagram form in Fig. 1-1.

Above 50 W or so, and especially in applications where low weight, size and high efficiency are essential, linear power converters become less attractive. The reason for this lies in the necessity for an expensive and heavy mains frequency transformer, which adds great weight and volume to the converter. Another reason is the inherently inefficient method of operation which results in high power loss in the linear regulator, and thus relatively high heatsink volume, especially if the input voltage range is wide and the output current is high. Above 50 W, switch-mode regulators are usually employed to give lighter, more compact power supply systems, because they operate at much higher power conversion efficiency and high internal switching-frequency, which allows the use of much smaller heatsinks and wound components.

The principle of operation of a SMPS (switch-mode power supply, see Fig. 1-2) can be briefly described as follows:
If the input voltage is supplied from the mains, it is directly rectified by a bridge rectifier and filtered to obtain a low ripple d.c. supply for the dc/dc converter. If the input source is already a d.c. voltage, it can be directly applied to the converter. This d.c. input voltage is switched at high frequency (usually above the audible frequency

range, >20kHz) and the output is regulated by varying the output pulse duty-ratio. The resulting pulsed voltage is then filtered to obtain the desired d.c. output voltage. A portion of the output voltage is taken as a feedback signal and compared with a stable voltage reference, V_{REF}. The error is used to regulate power switch conduction duty-ratio, via the controller and PWM modulator, to keep the output at the constant or varying demand level set by V_{REF}.

Over the last three decades, the rapid advances in electronic components miniaturization, especially in space and communication applications, have led to an ever increasing need for smaller size, lower weight and higher efficiency power converters. This requires the use of higher switching frequency (>100kHz) which allows smaller wound components, such as transformers and inductors, and also smaller filter capacitors to be used. Power conversion efficiency has also been improved by power device and circuit developments to allow heatsink volume to be similarly reduced. As a result of this, and the intensive research and development in switching power converter, tens of dc/dc and dc/ac converter topologies have been developed, each of which come with inherent problems. Therefore, each topology has certain applications and cannot be used in others. Some are used for high power, others for off-line applications and some are used when multiple output voltages are required. Therefore, before a dc/dc converter is designed, all or some of the following parameters should be considered to achieve the optimum design for a certain application:

Output power range, current and voltage ratings, isolation requirements, input voltage range, number and levels of output voltages, power loss and efficiency, output voltage ripple, voltage and current protection requirements, EMI, line and load regulation, stability, reliability, input current harmonics, weight, size and cost.

Attempts are continually being made to improve the performance of power converter topologies through looking at their main drawbacks and finding solutions to eliminate these or reduce their negative effects.

Switching power converters, in general, can be divided into two broad categories, namely isolated and non-isolated power converters.

Switching power converters, in general, can be divided into two broad categories, namely isolated and non-isolated power converters.

Non-isolated topologies, such as buck, boost, buck-boost and polarity inverting converters do not use power transformers for isolation purposes. In most of these topologies, the output and input grounds are the same, and are used in applications where the input voltage is within the safety range, i.e. <(60-70)V, or in applications where the user has no access to the output voltage, in which case no isolation is required even if the input and/or output voltages are outside the safety range. These topologies are not considered in this report.

Isolated switch-mode power converters, on the other hand, are the most common topologies and are extensively used in power electronics applications. The isolation between the input and output is required for the following reasons:

1. Most power converter circuits require multiple output voltages which may be different, have different polarities and/or referenced to different points in the circuit. In this case, the only isolation element to use is a transformer with multiple secondary windings.
2. Galvanic isolation is a safety requirement when power converters are operating from a 120-240 V mains supply. This is necessary to keep the low voltage outputs well away from the high voltage input and to allow the output to be earthed.
3. When the output voltages are widely different from the input voltage, basic non-isolated dc/dc converters are not used: they do not operate so efficiently or predictably under these conditions. In this case, the turns-ratio of the isolation transformer can be selected to obtain the desired outputs.

The only isolating element available in power applications is the transformer, despite the drawbacks resulting from its use, and the difficulties facing the designer when designing or modelling transformers. Although the birth of the transformer revolutionised electrical systems, a second and perhaps more important revolution will occur when the transformer disappears and is replaced by a small-size, low-

avoid or escape from fully understanding and mastering the function of the transformer. This starts from the basic principles of magnetism to magnetic core properties including non-linearity and saturation, to transformer design procedure, and finally to the construction of transformers, which plays a big role in switch-mode power supply behaviour.

Mastering transformer design and construction is not the only requirement which the designer confronts, but transformer modelling is another important and perhaps more difficult issue which is raised when isolated dc/dc converters simulation is considered. In this case, a full understanding of transformer non-linear behaviour, such as hysteresis and saturation, is required, especially if a numerical simulator such as MATLAB is used for circuit simulation. Therefore, the power converter designer should grasp the subject of transformer design, construction and modelling. The difficulty of modelling transformers stems from the fact that no single equation describing their behaviour exists, since each future flux density working point depends on, among other parameters, the history of the core, i.e. the previous working points.

This work makes a contribution to the study of the main and frequently used transformer-isolated converters and inverters, starting by highlighting some of their major drawbacks and suggesting solutions to these drawbacks in order to improve their performance, applying high-frequency techniques to transformer-isolated dc/ac inverters, and ending with a comparison of low- and high-frequency dc/ac inverters. In addition to examining transformer-isolated dc/dc and dc/ac converters practically, comprehensive simulation is used throughout this work to show typical waveforms and to verify the validity of the presented solutions to the existing problems. Therefore, particular attention has been paid to single- and three-phase transformer function and modelling in PSPICE and MATLAB.

A statistical analysis of switching power supply design process has suggested that 50% of electrical faults that are discovered during the product realization process could be detected by circuit simulation [1]. Errors can be corrected before the

A statistical analysis of switching power supply design process has suggested that 50% of electrical faults that are discovered during the product realization process could be detected by circuit simulation [1]. Errors can be corrected before the prototype is developed, thus eliminating a non-value-added design iteration. Simulation provides a means of understanding new developments and comparing them with existing methods. Oversimplifying simulated circuits often gives results which are usually far from reality. Overcomplicating them, on the other hand, gives very accurate results, but has the disadvantages of complexity and long simulation time. Therefore, careful judgment should be exercised in selecting the complexity of the simulated circuit such that it gives sufficiently realistic waveforms to understand the new improvement within an acceptable computation times, and without a need for lengthy empirical data collection.

This report has been divided into several chapters to simplify understanding the contents of the work.

Chapter Two presents a brief introduction to some of the transformer-isolated switch-mode power converter topologies. This includes push-pull, flyback, half-bridge and full-bridge circuits. This chapter helps to understand the principle of operation of each topology, by showing the main circuit diagrams and typical waveforms, and then highlights the main drawbacks of each topology. Forward converters, including single-ended, double-ended and interleaved forward converters, have been studied separately in Chapter Three. In this chapter, the effect of the reset-winding turns on the peak primary-current and voltage stress on the power switches in single-ended forward converters has been analyzed and supported by new graphs. A method of eliminating the drive transformer from double-ended forward converters is first simulated and then practically tested. The effect of the output voltage and load current on the limitations of this method is also discussed.

Chapter Four discusses the main problems in push-pull dc/dc converters, in particular the major shortcoming of flux imbalance which is usually encountered in these

While considering push-pull circuits, a study is conducted in Chapter Five to examine the use of three-phase transformers in push-pull dc/dc converters, in an attempt to utilize the advantages of the three-phase transformers. The limitations of this new topology are discussed and a conclusion of using such technique in dc/dc converters is drawn.

Chapter Six presents high-frequency dc/ac inverters as alternatives to the low-frequency inverters which use bulky laminated steel transformers. The high-frequency dc/ac inverter technique has been applied to the converter topologies discussed in Chapters Two and Three. Power-device current and voltage ratings have been evaluated for each low- and high-frequency inverter topologies.
Power-semiconductor switch and diode power-losses, i.e. switching and conduction power-losses, have been estimated for all the dc/ac inverter topologies in Chapter Seven, which gives design examples for different dc/ac inverters using low- and high-frequency techniques.

As a result of this study, it has been shown that low- and high-frequency full-bridge inverters offer the maximum efficiency compared to all other topologies. A low-frequency full-bridge inverter, therefore, was designed and thoroughly investigated in Chapter Eight. The effect of *dv/dt* on the power switches, which is one of the main reasons that causes switch failure in these inverters has been studied. In this chapter, a special section has been devoted to study the effect of the snubber resistor values in full-bridge inverters and converters on the power loss in these resistors. The effect of transformer interwinding capacitance is also investigated, and a method to reduce this effect is first simulated and then applied to the inverter.

Chapter Nine presents the effect of the main parasitic elements, such as stray and magnetizing inductance, ESR (equivalent series resistance of capacitors), on the performance of switch-mode power converters, and describes how these effects can be reduced. An ESR measurement circuit has been designed, constructed and is briefly discussed.

Comprehensive circuit simulation using PSPICE was conducted for almost all dc/dc and dc/ac converters studied in this work, during which a lot of experience in simulating electrical circuits, especially switching power circuits, was gained. To make it easier for other PSPICE users, PSPICE problems have been highlighted in Chapter Ten, and methods for eliminating or reducing these problems have been examined. The MATLAB dynamic system simulator is suggested as an alternative to PSPICE in some situations where PSPICE is more difficult to use. The advantages of MATLAB compared to PSPICE in such cases are also presented.

Since this work primarily concentrates on transformer-isolated switch-mode power converters, much time has been spent on single- and three-phase transformer modelling to help with simulating transformer-isolated power converters. The most important and difficult part is core hysteresis modelling in MATLAB which is discussed in Chapter Eleven. Chapter Twelve discusses PSPICE and MATLAB single-phase transformer modelling, and shows the effect of remanent flux in transformers and how the steady-state flux can be quickly established when simulating single- and three-phase transformers in PSPICE.

After modelling single-phase transformers in MATLAB, simulation of transformer-isolated dc/dc converters in MATLAB have been discussed in Chapter Thirteen. Since three-phase transformers have the advantages of reduced size and weight and, hence, less cost over three single-phase transformers that have the same power capabilities, Chapter Fourteen is devoted to three-phase transformers operation and modelling. Equations are derived to calculate material saving when these transformers are used, and examples of different core geometries are given.

Chapter Fifteen is devoted to thermal modelling which is an important issue in switching power supplies. In order to model the junction and case temperature of power semiconductors, accurate voltage and current waveforms should be obtained by simulation. Therefore, MOSFET non-linear capacitances have to be properly modelled, together with the thermal impedance properties of these semiconductors

which are specified in the data sheets. Core loss modelling, including hysteresis and Eddy-current losses, are also described.

Chapter Sixteen presents the conclusion and further work, followed by the appendices and references which are placed in Chapter Seventeen.

CHAPTER ONE REFERENCES

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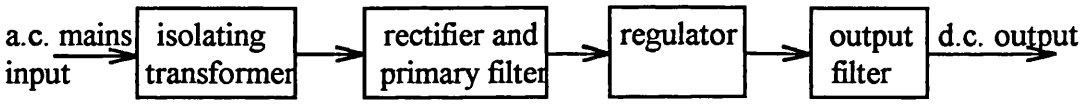


Fig. 1-1 A block diagram for the linear power supply

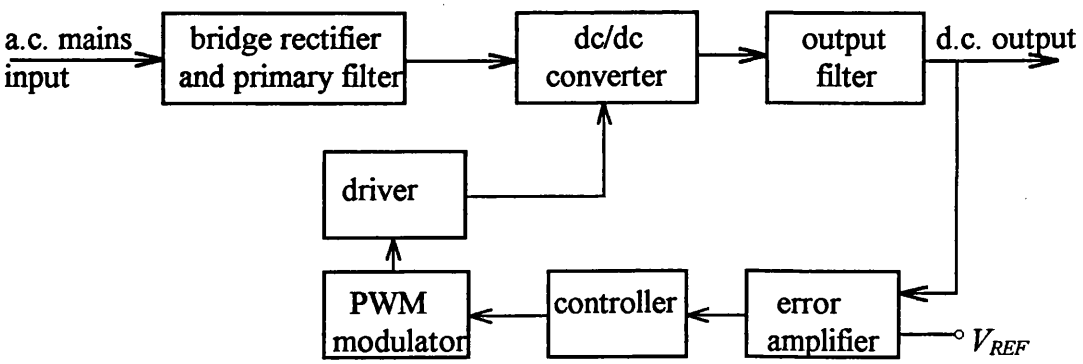


Fig. 1-2 A block diagram for a switch-mode power supply

TRANSFORMER-ISOLATED DC/DC CONVERTERS

2-1 INTRODUCTION

This chapter, as well as Chapters Three and Four, describe the principle of operation of the main and frequently-used transformer-isolated dc/dc converters and considers some of their major drawbacks in order to investigate improving their performance. These chapters form the basis to Chapters Six, Seven and Eight which thoroughly investigate dc/ac inverters that use dc/dc converters as the milestone to their operation.

2-2 PUSH-PULL CONVERTERS

Push-pull dc/dc converters are amongst the oldest topologies used for power conversion [1]. This section reviews the principles of operation of these converters and their advantages and disadvantages. This will help in understanding Ch. 4 which studies flux imbalance especially in push-pull converters.

A more complete analysis of the circuit, supported by equations and confirmed by PSPICE simulation, gives a better understanding to the circuit operation and core flux change during circuit dead times, where the magnetising inductance resets very slowly as the transformer magnetising current circulates in low-voltage loops.

2-2-1 Principle of Operation

Fig. 2-1 shows the power stage of a push-pull converter. It consists of a power transformer and two power switches which are turned "on" and "off" alternately. The conduction duty-cycle of the power switches, and hence the output pulse width, is determined by the control circuit to keep the output voltage constant. Each transformer primary winding voltage pulse, or voltage-time integral, during the two transistor conduction periods should be identical, otherwise the transformer core moves into saturation. In consequence, the current in one or more of the transistors may not be properly reset and over several cycles transistors may be destroyed. Typical operating waveforms for a push-pull converter are given in Fig. 2-2 and will now be discussed. The following analysis assumes that the circuit has been operating for some time and reaches a steady-state, and that the circuit is operating with close-to-ideal devices and components.

2-2-1-1 Q_1 Turn-on

Q_1 is first turned "on" assuming that the flux density is at point X of the hysteresis loop, as shown in Fig. 2-3. When Q_1 is turned "on", the voltage across the first primary is: $v_{P1} = V_{DC} - 1$, where the on-state voltage of all power switches, V_{QO}, is assumed relatively constant at 1 V. This voltage v_{P1} will be transferred to the secondary such that $v_{S1} = v_{P1} \cdot \frac{N_S}{N_P}$, where N_P and N_S are the primary and secondary turns, respectively . If the voltage drop across the secondary rectifier diode is approximately constant at 0.7 V, then:

$$v_F = v_{S1} - 0.7 = v_{P1}\frac{N_S}{N_P} - 0.7 = (V_{DC} - 1)\frac{N_S}{N_P} - 0.7 \qquad (2\text{-}1)$$

If T_{ON} is the power MOSFET conduction time, T_S is the duration of one cycle (i.e. $1/f_{SW}$, where f_{SW} is the switching frequency), then the output voltage, which is the average of the input of the LC filter, will be:

$$V_O = \frac{2T_{ON}}{T_S} v_F = \frac{2T_{ON}}{T_S}\left[(V_{DC} - 1)\frac{N_S}{N_P} - 0.7\right] \qquad (2\text{-}2)$$

where two pulses exist in each cycle. In a practical system, negative feedback is used to adjust T_{ON} to maintain a constant output voltage despite load current and line voltage variations, and changes in other operating conditions and components.

At Q_1 turn "on", diode D_1 conducts the load current, I_L, as shown in Fig. 2-2, which is assumed to be constant because of the large filter inductor, L. The voltage across Q_1 will be V_{CEsat} if bipolar transistors are used, or $R_{DSon}\, i_P$ if MOSFET's are used [1-4 V is a practical "on" voltage for power devices].

Since the dot end of P_1 is almost V_{DC} higher than the no-dot end, the dot end of P_2 is also higher by the same amount than the no-dot end of P_2, Q_2 is subjected to and must block $2V_{DC}$. Therefore, the switches in push-pull converters must withstand at least twice the d.c. applied voltage plus some value to allow for the additional turn-off spikes due to the transformer leakage inductance. This additional value is assumed to be about 30% of the d.c. voltage.

D_2 in this case is subjected to a reverse voltage and it stays "off" as long as Q_1 is "on".

During this "on" time, magnetising current is built up in primary P_1, which is given by:

$$i_M = \frac{1}{L_M}\int v_{P1}\, dt \qquad (2\text{-}3)$$

At the end of the Q_1 "on" pulse, i_M reaches a peak value, $\hat{i}_M$, as shown in Fig. 2-2, and the flux density reaches point Y on the hysteresis loop, as shown in Fig. 2-3.

2-2-1-2 Q_1 Turn-off

When Q_1 is turned "off", there is no primary current since both switches are now "off". The energy stored in the large filter inductor forces D_1 and D_2 to conduct and share the load current. Point F, therefore, goes negative just enough for D_1 and D_2 to conduct. Practical values of this voltage is -0.3 to -1.5 V depending on the load current and the type of the rectifier diodes.

Ideally, ignoring for the moment the magnetising current, D_1 and D_2 conduct exactly the same current, which is $I_L/2$. In this case, the voltage drop across each diode will be the same. Since both diodes conduct the same current, the flux produced by the upper-going current is equal to the flux produced by the lower-going current. Hence there is no change in the core-flux during this phase of the cycle and it remains at the value produced by $\hat{i}_M$.

In practice, to maintain this flux, a current equals to $\hat{i}_M$ must flow in the primary, or a reflected version of it, i.e. $\hat{i}_M N_P / N_S$, should flow in the secondary. But since no primary path exists, this current flows in the secondary in such a direction to keep the flux flowing in the same direction. In other words, examining the transformer model of Fig. 2-4, it can be seen that at Q_1 turn-off, the magnetising current flows out of the dot end of P_1, or, alternatively, into the dot end of secondary S_1 or S_2 as shown by the arrows in Fig. 2-4.

Recalling that the load current is assumed constant at I_L, any increase in i_{D2}, due to the magnetising current, causes the same decrease in i_{D1} such that, during the dead time, the following formula is satisfied:

$$i_{D1} + i_{D2} = I_L \tag{2-4}$$

$$(\frac{I_L}{2} - i_{M1}) + (\frac{I_L}{2} + i_{M2}) = I_L \tag{2-5}$$

which yields:

$$i_{M2} = i_{M1} \tag{2-6}$$

Also, since the ampere-turns of the primary must equal that of the secondary, the following equations can be written (recall that $N_{S1}=N_{S2}=N_S$ and $N_{P1}=N_{P2}=N_P$):

$$N_{P1}\hat{i}_M = N_{S1}i_{M1} + N_{S2}i_{M2} \tag{2-7}$$

$$N_{P1}\hat{i}_M = N_S(i_{M1} + i_{M2}) \tag{2-8}$$

$$\hat{i}_M = \frac{N_S}{N_P}(2i_{M1}) \tag{2-9}$$

which gives :

$$i_{M1} = i_{M2} = \frac{1}{2}\frac{N_P}{N_S}\hat{i}_M \tag{2-10}$$

Therefore, during the dead time, the following may be written:

$$i_{D1} = \frac{I_L}{2} - \frac{1}{2}\frac{N_P}{N_S}\hat{i}_M \tag{2-11}$$

$$i_{D2} = \frac{I_L}{2} + \frac{1}{2}\frac{N_P}{N_S}\hat{i}_M \tag{2-12}$$

Because different currents flow in each diode, the voltage drop across one diode will be slightly different from that across the other. Namely, the voltage at point D, v_D, in Fig. 2-4 will be higher than the voltage at point E, v_E. Also, these two voltages must be equal in amplitude and opposite in direction, since they are voltages across two windings having the same number of turns and wound on the same core. Therefore, v_D will be positive and v_E will be negative by a small amount that is just enough to allow for the difference between the two diode currents and diode voltage drops.

Because the very small secondary voltages at points D and E are also small when reflected to the primary, e.g. $N_P/N_S\ v_D$, the magnetising inductance, L_M, resets very slowly during the dead time. Therefore, since di_M/dt is low, the rate of change of core flux is also low and may be considered constant. Hence, the flux density virtually remains at point Y on the hysteresis loop during this period.

The very low reflected voltage across the primary during the dead time, results in approximately V_{DC} across the off-state switches.

At the instant of Q_1 turn-off, the energy stored in the series-connected transformer-primary leakage-inductance causes an overshoot on the drain of Q_1 as its output capacitance charges, as seen in Fig. 2-2. The low output capacitance rapidly discharges to V_{DC}.

2-2-1-3 Q_2 Turn-on and Turn-off

After the dead time, Q_2 is turned "on" and the core flux moves from point Y on the hysteresis loop back to point X (assuming symmetrical operation), and the same

discussion for Q_1 now applies for Q_2 at turn-on and turn-off with Q_2 and D_2 replace Q_1 and D_1.

2-2-2 PSPICE Push-Pull Converter Simulation

A push-pull converter as shown in Fig. 2-5 was simulated in PSPICE to confirm the above analysis. Fig. 2-6a shows i_{D1} and i_{D2} together with the primary current reflected to the secondary, i'_P, which gives a trapezoidal primary current waveform. The ramp of this waveform approximates to the magnetising current, and the step approximates to the constant load current. The difference between i'_P and i_{D1} at turn-off (about 12.1 μs) is $\hat{i}_M$, which is the same as the difference between i_{D2} and i_{D1} during the dead time, (12.1-13.1) μs. Also seen is that i_{D1} and i_{D2}, during the dead time, are as given in Eq's (2-11) and (2-12), i.e. i_{D2} is higher than i_{D1} by $\hat{i}_M$. Fig. 2-6b shows the voltage drop across D_1 and D_2, and the flux density. During the dead time, there is virtually no change in the flux density. The two voltage drops across the diodes seem to be identical, but cursor information shows that v_{D2} is slightly higher than v_{D1} (≈ 24 mV in the simulated example).

2-2-3 Advantages of Push-Pull Converters

1. Multiple outputs may be produced if multiple secondary windings are used.
2. Each of the floating outputs may be referenced to any point in the circuit for positive or negative supplies.
3. Full utilisation of the core is possible. Therefore, higher power than with forward converters can be transformed for a given transformer provided the extra winding can be fitted.
4. Since only one power switching device is in series with the primary, total conduction and switching losses are lower compared to full-bridge converters.

2-2-4 Disadvantages of Push-Pull Converters

1. Power switches are subjected to at least twice the d.c. voltage plus some value to account for any voltage spike due to leakage inductance.
2. Due to point 1 above, push-pull converters are not favoured for off-line applications.
3. Flux imbalance due to asymmetry in transformer operating conditions may cause saturation. For more details on flux imbalance, refer to Ch. 4.
4. The primary utility factor of the transformer is not as good as in half- and full-bridge converters, because half of the primary is used at a time.

2-3 BUCK-BOOST FLYBACK CONVERTERS

2-3-1 Principle of Operation

Fig. 2-7 shows the simplified power section of a flyback converter, where a rectified voltage, V_{DC}, is applied to the primary winding of a transformer. The circuit uses one switching device, Q, and a switching frequency with a pulse width modulation, PWM, to maintain the d.c. output voltage constant.

When the transistor Q is turned "on", the start of both windings go positive. Diode D, will be reverse-biased and blocks the reflected primary voltage. Hence, current will not flow in the secondary during this phase of operation. During this period, a current builds up in the primary, while the secondary is treated as an open circuit. Therefore, the primary can be considered as an inductor, and the current will increase according to $\frac{di_p}{dt} = \frac{V_{DC}}{L_P}$, where V_{DC} is the applied voltage, L_P is the primary inductance. For a first-order approximation, V_{DC} and L_P are assumed constant. Therefore, primary current will increase linearly as shown in Fig. 2-8a. The flux

density B in the core will increase from B_r, the residual flux density, to B_W, the peak working flux density, making a change of $\Delta B = B_W - B_r$ as shown in Fig. 2-8b.
At the end of the "on" period, Q is turned "off", and the primary current drops to zero. This causes the flux density to reverse to B_r making a change of - ΔB. Since this change in the flux density is negative, the voltage will reverse on all windings. During this period, the rectifier diode D conducts and the current flows now in the secondary in the same direction, i.e. from the start of the winding to the end, with a magnitude defined by the turns ratio. The secondary current starts from a value of $\hat{i}_S = \hat{i}_P / N$, where $\hat{i}_S$ is the peak secondary current, $\hat{i}_P$ is the peak primary current, and N is the turns ratio $N = N_S / N_P$. Since there is no primary current, the primary circuit can be considered as an open circuit. Therefore, the secondary current will decrease at a rate defined by $\frac{di_S}{dt} = \frac{v_S}{L_S}$, where v_S is the secondary voltage, and L_S is the inductance of the transformer referred to the secondary. Fig. 2-9 shows the current waveform and the magnetisation during the "off" period. If the secondary current reaches zero, i.e. all energy which was stored in the transformer during the "on" period is transferred to the load, before the next "on" period, the circuit is said to be operating in a complete energy transfer mode or Discontinuous Conduction Mode, DCM. This means that there is a period when the primary and the secondary conduct no current, and the load is fed from the storage capacitor C. If the next "on" period starts before the secondary current falls to zero, i.e. some of the energy which was stored in the transformer is not completely transferred, and the circuit is said to be operating in an incomplete energy transfer mode or Continuous Conduction Mode, CCM. In this case, the flux density is as shown in Fig. 2-10.

2-3-2 Advantages of Flyback Converters

1. The transformer used in the flyback converter combines the action of an isolating transformer, an output inductor, and a freewheeling diode. As a result, the circuit provides extremely cost-effective and efficient stabilised d.c. outputs.
2. The technique is useful for multiple-output applications, where several semi-stabilised outputs are required from a single supply.

2-3-3 Disadvantages of Flyback Converters

1. In incomplete energy transfer, there is a "right-half-plane zero" in the transfer function, which introduces an extra 180° of phase shift at high frequency. This can cause instability, and make flyback converters very difficult to design. Therefore, the loop stability must be checked for both modes of operation.
2. High ripple currents flow in the transformer and output components. Therefore, the efficiency is reduced. As a result of this, flyback converters are usually restricted to power levels below 150 W.
3. It is rather more difficult to design transformers for application in flyback converters than in push-pull converters since they are required to:
   - Store energy.
   - Give electrical galvanic isolation.
   - Provide current-limiting inductance.
   - Support a considerable d.c. current component.
4. The voltage across the power switch is higher than V_{DC}, $(\frac{N_P}{N_S}V_O + V_{DC})$.

2-4 DIAGONAL HALF-BRIDGE FLYBACK CONVERTERS

2-4-1 Principle of Operation

Fig. 2-11 shows the diagonal half-bridge (two-transistor) double-ended flyback converter. The supply voltage V_{DC} is applied across the transformer primary through two power switches Q_1 and Q_2, which are driven by the control circuit such that they will both be either "on" or "off" together, as in double-ended forward converters. When they are "on", D_3 blocks the negative voltage induced at the secondary. In this case, the primary stores energy. When they are "off", flyback action takes place, and D_3 conducts, and energy is transferred to the load.

Since two switches are used, a small drive transformer is required. D_1 and D_2 return leakage inductance and excess flyback energy to the supply lines when Q_1 and Q_2 are "off", and provide hard voltage clamping for Q_1 and Q_2 such that the reverse voltage across the switches is only two diode drops above the supply-line voltage. These two diodes eliminate the need for the energy recovery winding or snubbing components.

2-4-2 Advantages of Diagonal Half-Bridge Flyback Converters

1. The voltage across the power devices can not exceed the supply voltage by more than one diode drop.
2. The energy stored in the primary leakage inductance is largely returned to the supply line and is not lost. However, the reset current circulation does slightly increase converter power-loss.
3. Any excessive energy stored in the transformer in the previous "on" period, will be returned to the supply line at the beginning of the next flyback "off" period.
4. No need for energy recovery winding or snubbing components. Therefore the cost is less.

2-4-3 Disadvantages of Diagonal Half-Bridge Flyback Converters

1. Two power switches are used.
2. Due to the above disadvantage, an isolated drive circuit is required for the upper power switch.
3. Fast-action clamping diodes are required.

2-5 INTERLEAVED FLYBACK CONVERTERS

2-5-1 Principle of Operation

Interleaved flyback converters, as shown in Fig. 2-12, consist of two discontinuous-mode flyback converters. Power switches Q_1 and Q_2 are turned "on" alternately, and the secondary currents i_{S1} and i_{S2} are summed through D_1 and D_2. When Q_1 is turned "on", T_1 stores energy and i_{S1} is terminated since D_1 blocks the negative voltage now induced on N_{S1} . During the storage phase of T_1, T_2 is in a flyback phase (energy transfer phase). At the end of the "on" period of Q_1, T_1 transfers energy to the load together with T_2 as can be seen in Fig. 2-13. When the conduction period of Q_2 starts, i_{S2} is terminated and only i_{S1} feeds the output circuit.

This type of converters can work at power levels up to 300 W, where a single discontinuous-mode flyback converter cannot work because of the high primary and secondary currents.

2-5-2 Advantages of Interleaved Flyback Converters

1. Higher output power compared to normal flyback converters.
2. Since the circuit operates in a discontinuous-mode, response to load variations is faster, error amplifier band-width is higher, and feedback loop stabilisation difficulty is reduced.

2-5-3 Disadvantages of Interleaved Flyback Converters

More components are used and, hence, higher volume and cost due to the added flyback circuit.

2-6 PUSH-PULL DUTY-RATIO CONTROL HALF-BRIDGE CONVERTERS

2-6-1 Principle of Operation

Fig. 2-14 shows the power section of the half-bridge push-pull converter, which is used for direct-off-line switch-mode power supplies.

Because of the large storage capacitors C_1 and C_2, point A always has a value of almost $V_{DC}/2$. Thus, when Q_1 is turned "on", current flows from the positive rail through Q_1, the primary, and C_2 to the negative rail. When Q_2 is turned "on", current flows from the positive rail through C_1, the primary, and Q_2 to the negative rail. Therefore, the current flows in the primary in an opposite direction to that in the first half cycle, and a square wave is produced across the primary with an amplitude of $V_{DC}/2$ minus one voltage drop across the power switch when it is "on" (1- 4 V). This square wave is transferred to the output circuit by the turns ratio such that $v_S \approx \frac{N_S}{N_P} \cdot \frac{V_{DC}}{2}$. C_3 is used to prevent the problem caused by flux imbalance if the primary winding volt-second integral across the primary in one half cycle is different from that in the other half cycle (see Ch. 4 for more details on flux imbalance). D_1 and D_2 clamp the voltage spike due to the leakage and primary inductances.

When Q_1 is "on", D_3 conducts, and when Q_2 is "on", D_4 conducts. During the dead time, when both transistors are "off", both diodes are brought into conduction as freewheeling diodes. The dead time is varied by the control circuit to regulate the output voltage in the presence of changes in line voltage and load current, primarily, and should be longer than the maximum possible turn-off time of any power switch. Fig. 2-15 shows primary current and voltage waveforms for the circuit of Fig. 2-14.

2-6-2 Advantages of Push-Pull Half-Bridge Converters

1. Reduced voltage stress on power switches makes these converters the preferred topology for direct-off-line SMPS.

2. The capacitors used for filtering and input storage, are also used to supply one half of the bridge.
3. Primary leakage inductance spikes are clamped to V_{DC} by the clamping diodes D_1 and D_2, and the energy stored in the leakage inductance is returned to the supply line and not lost.

2-6-3 Disadvantages of Push-Pull Half-Bridge Converters

1. Using two power switches requires an isolated power-transistor drive transformer.
2. Power dissipation is higher because of the added power switch.
3. The main converter current must pass through the blocking capacitor which in consequence must have a high ripple current rating.
4. Transformer is driven by half the supply voltage rather than the full V_{DC} level. Hence, transformer primary-winding current is double that of the full-bridge converter.

2-7 PUSH-PULL FULL-BRIDGE CONVERTERS

2-7-1 Introduction

The full-bridge push-pull converter power stage has four power switches compared with two in half-bridge ones. Fig. 2-16 shows the power section of a typical full-bridge converter. Because four power switches and a drive transformer are used, full-bridge converters are more expensive than half-bridge and flyback converters. Therefore, they are used only at power levels of more than 1 kW.

2-7-2 Principle of Operation

As seen in Fig. 2-16, when Q_1 and Q_3 are turned "on" simultaneously, the current flows from the positive rail through Q_1, to the primary of T_1, and down through Q_3 to the negative rail. This makes the left end of the primary positive with respect to the right end. After the conduction time of Q_1 and Q_3, and before Q_2 and Q_4 are turned "on", all switches are held "off" for a time called the dead time. This is to insure that Q_1 and Q_3 are "off" before Q_2 and Q_4 are allowed to be "on". By doing so, cross conduction of four switches is avoided. After the dead time, Q_2 and Q_4 are turned "on" and the current flows from the positive rail through Q_4 to the primary and then through Q_2 to the negative rail. This makes the right end of the primary positive with respect to the left end. Therefore, the primary voltage will be as shown in Fig. 2-17, and the secondary voltage has the same waveform except it is scaled by the turns ratio.

The primary current consists of two components; the first is the magnetising current i_M which is determined by the magnetising inductance value and the applied voltage level, and therefore has a ramp form; the second is the load current reflected to the primary which has a step form. Therefore, the primary current waveform has a trapezoidal form as shown in Fig. 2-17.

Fig 2-18 shows some practical waveforms showing the effect of the magnetising and leakage inductance.

The function of the diodes D_1-D_4 is as follows:

At the end of the conduction time of Q_1 and Q_3, all diodes are "off". The energy stored in the primary leakage inductance, forces the drain voltage of Q_3 to increase and the source of Q_1 to decrease. When the drain voltage of Q_3 reaches one diode drop above the positive rail, D_4 conducts and clamps the voltage. At the same time, the source of Q_1 (the drain of Q_2) is clamped by D_2 to a one diode drop below the negative rail. Therefore, power switches Q_1 and Q_3 will not be subjected to more than one diode drop above the d.c. voltage. The same is applied for diodes D_1 and D_3, and switches Q_2 and Q_4.

The snubber pairs C_1R_1, C_2R_2, C_3R_3 and C_4R_4, are used to reduce the turn-off stress on the power devices by providing an alternative path for the drain current during the turn-off transient.

2-7-3 Advantages of Full-Bridge Converters

1. The maximum voltage applied across the power switches is nearly equal to the d.c. voltage. Therefore this type of converters is suitable for off-line applications.
2. Because in each half cycle, the full d.c. voltage is applied across the primary, and because full-wave output rectification is employed, an excellent utility factor for the transformer core and windings is provided.
3. Also, because the full d.c. voltage is applied across the primary compared with half the d.c. voltage in half-bridge converters, primary current is half for the same output power. Therefore, the output power available from full-bridge converters is double that in half-bridge ones with increasing primary current.
4. No need for a resetting winding as required in forward converters.

2-7-4 Disadvantages of Full-Bridge Converters

1. Because four power switches are used, full-bridge converters are more expensive compared with half-bridge ones.
2. As in half-bridge converters, an isolating transistor drive transformer is required especially when bipolar transistor switches are used. This adds extra cost and complexity.
3. Since two power switches are always in series, on-state losses tend to be higher than two-transistor circuits.

CHAPTER TWO REFERENCES

1. Keith Billings, "Switchmode power supply handbook", McGraw-Hill Inc., New York, 1989.

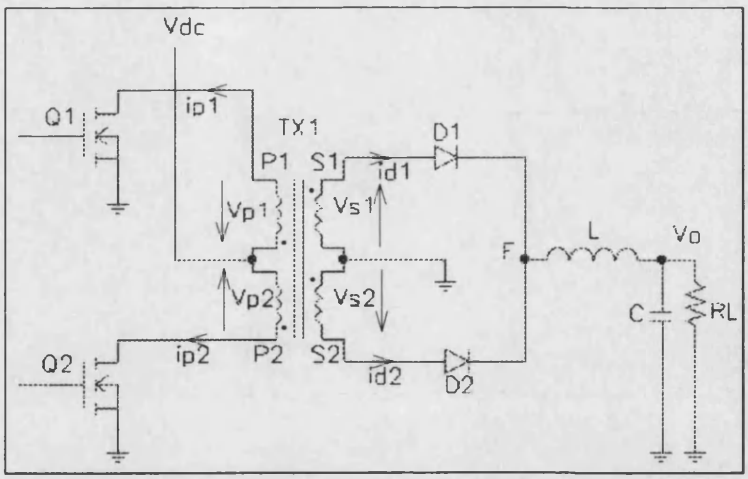


Fig. 2-1 The power stage of a push-pull dc/dc converter

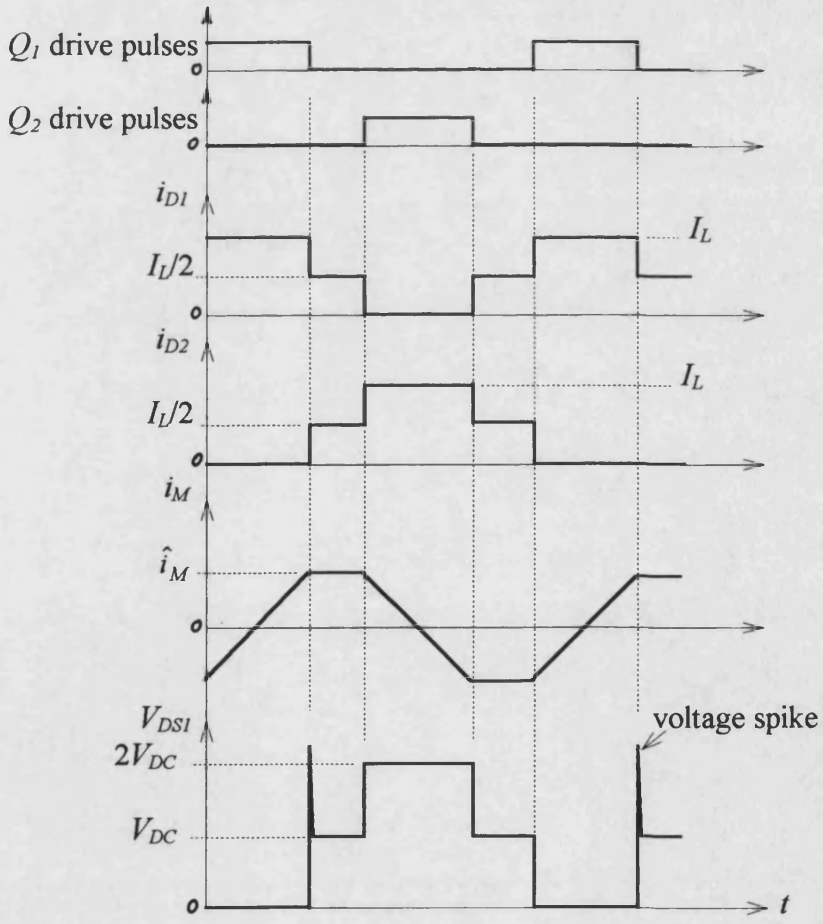


Fig. 2-2 Typical voltage and current waveforms for push-pull converters

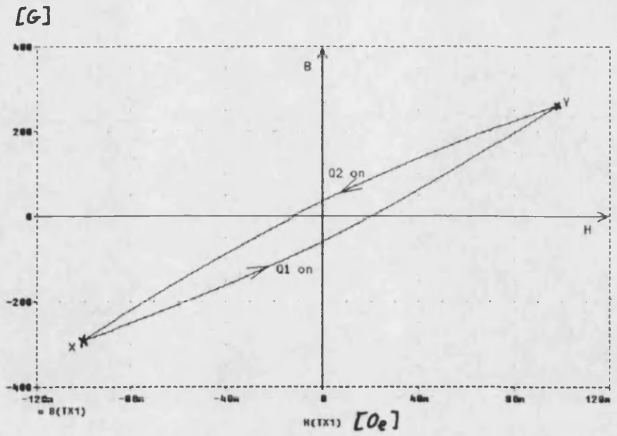


Fig. 2-3 The hysteresis loop of a core used in push-pull dc/dc converters

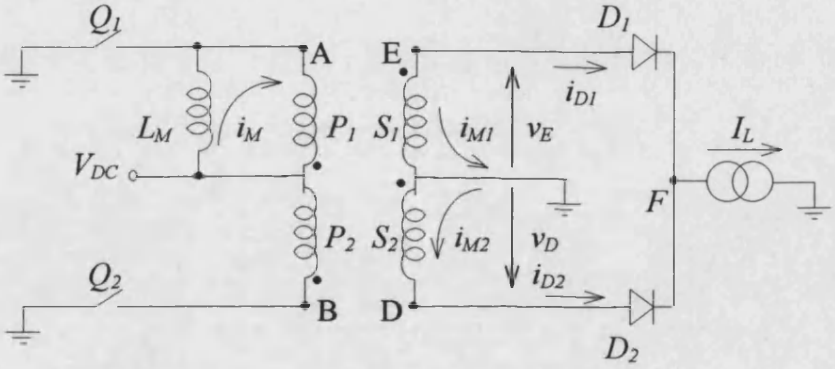


Fig. 2-4 Primary P_1 is simulated by its equivalent circuit to show the direction of the magnetising current during the dead time

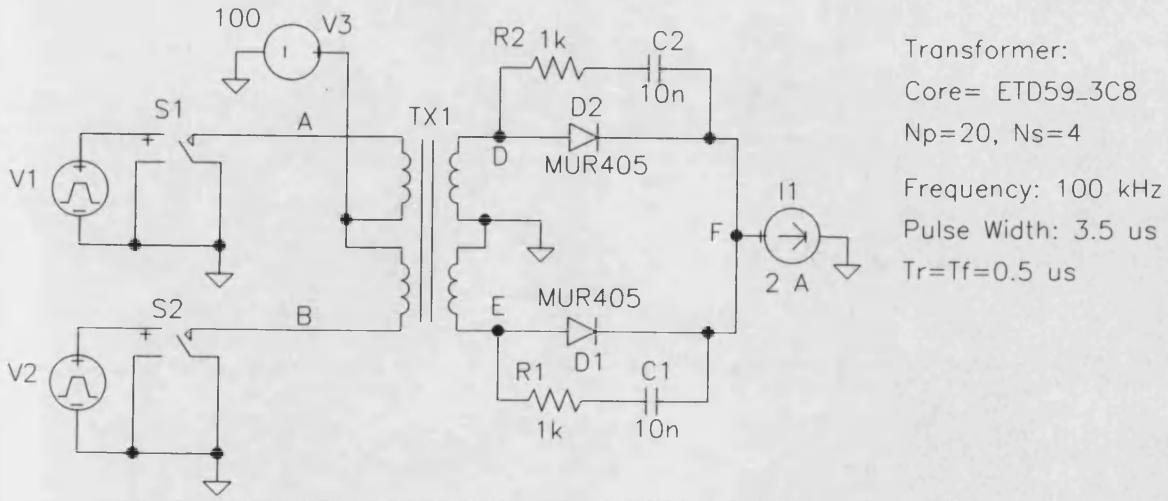


Fig. 2-5 A circuit used to simulate the push-pull converter in PSPICE

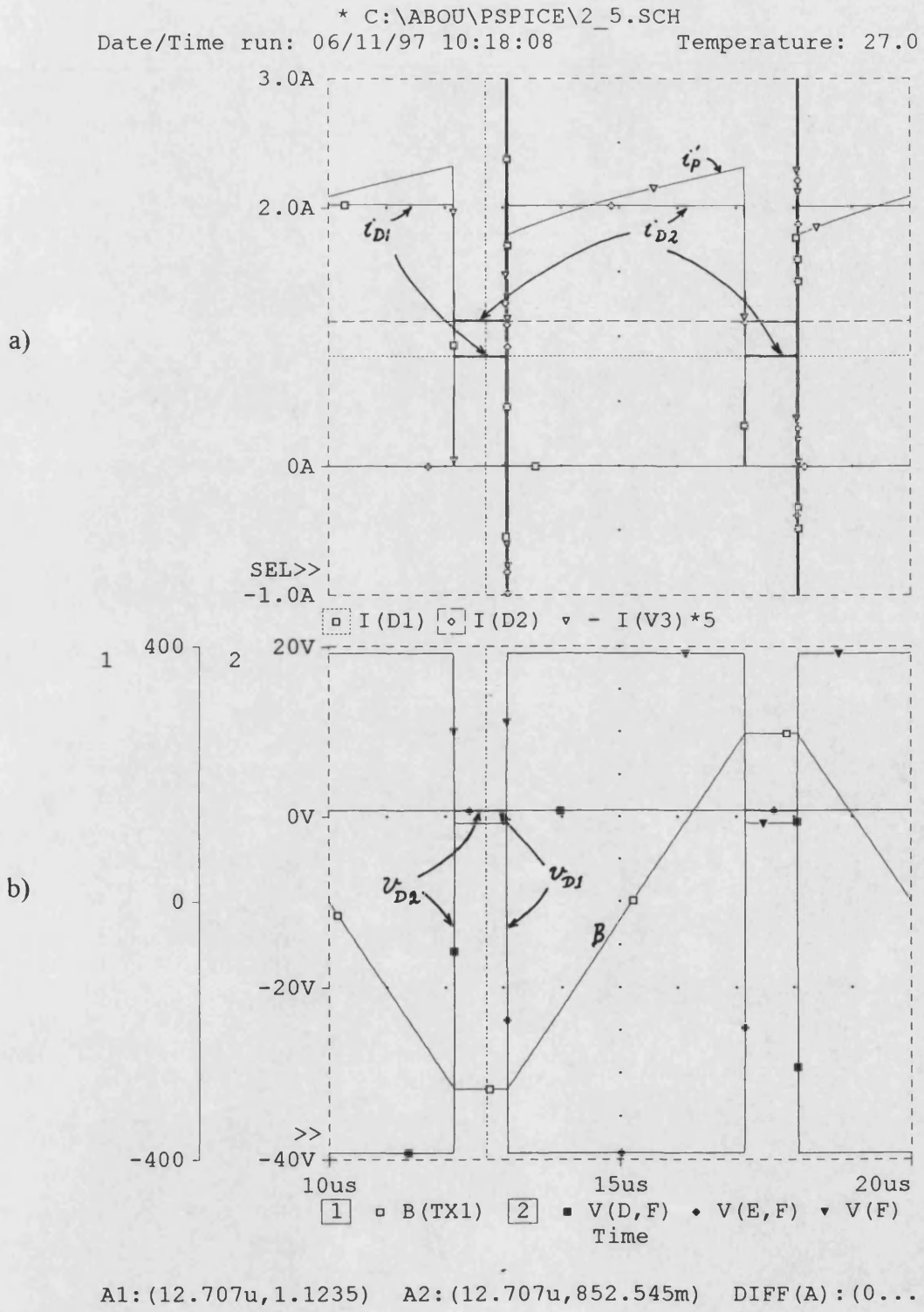


Fig. 2-6 a) Transformer primary and secondary currents and b) core flux density and voltage drop across the rectifier diodes

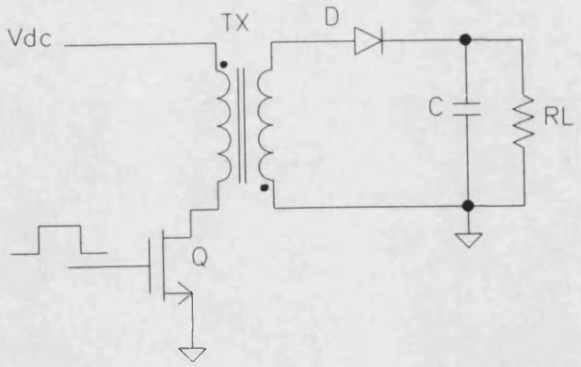
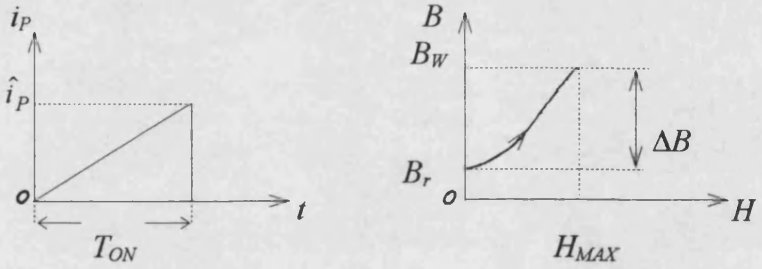
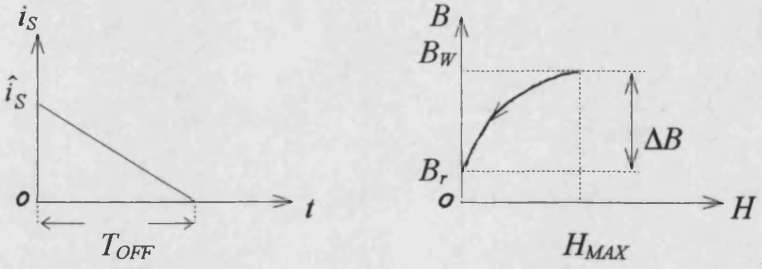


Fig. 2-7 The power stage of a flyback converter



(a) (b)

Fig. 2-8 a) The primary current and b) the flux density during the switch turn-on



(a) (b)

Fig. 2-9 a) The secondary current and b) the flux density during the switch turn-off

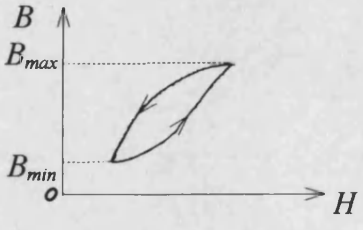


Fig. 2-10 The flux density in CCM

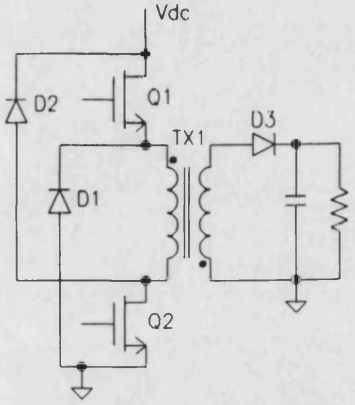


Fig. 2-11 The power stage of the diagonal half-bridge flyback converters

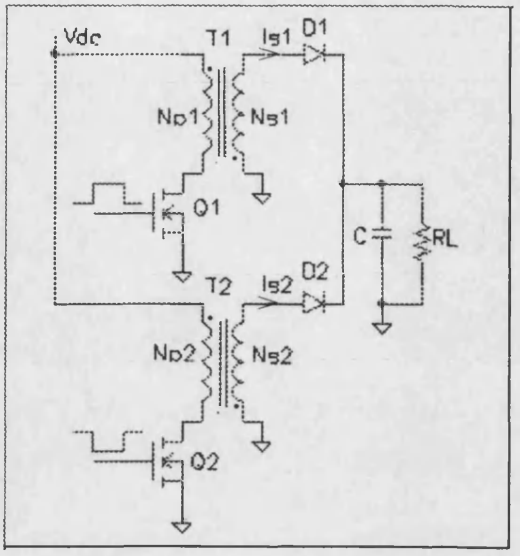


Fig. 2-12 The power section of an interleaved flyback converter

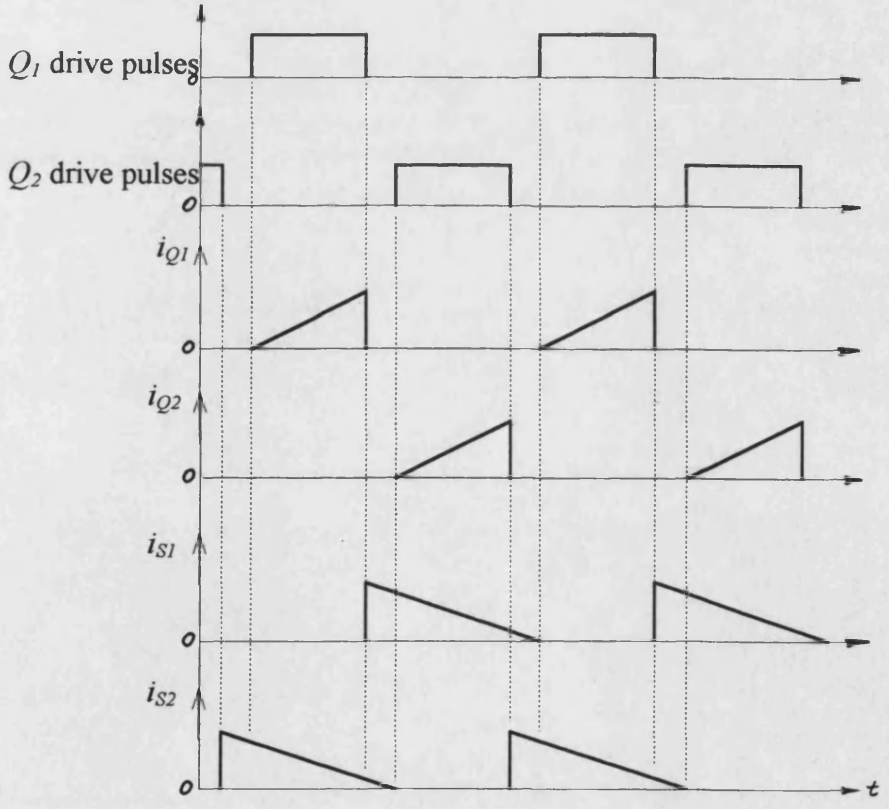


Fig. 2-13 Typical waveforms for interleaved flyback converters

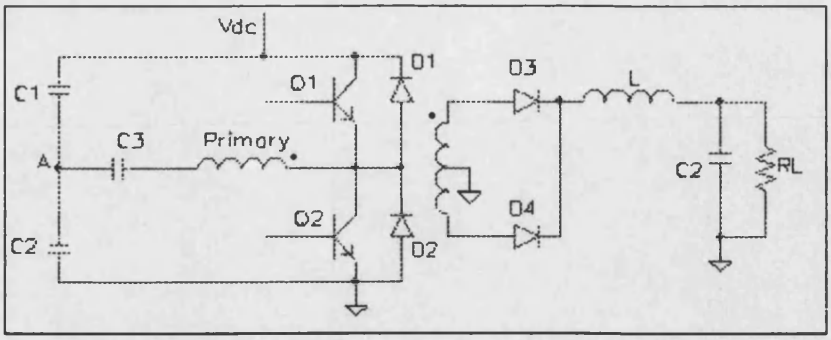


Fig. 2-14 The power section of a push-pull half-bridge converter

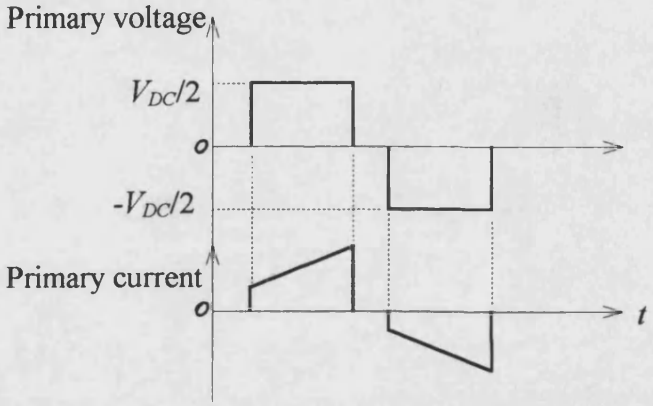


Fig. 2-15 Primary voltage and current for the half-bridge converter

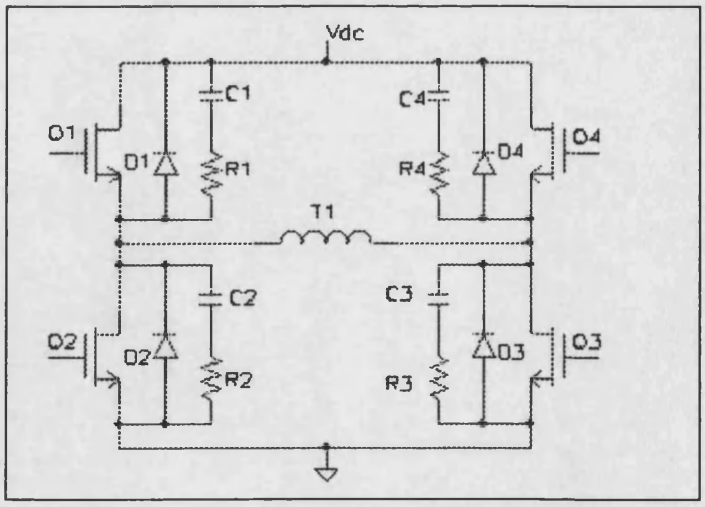


Fig. 2-16 The power section of a full-bridge converter

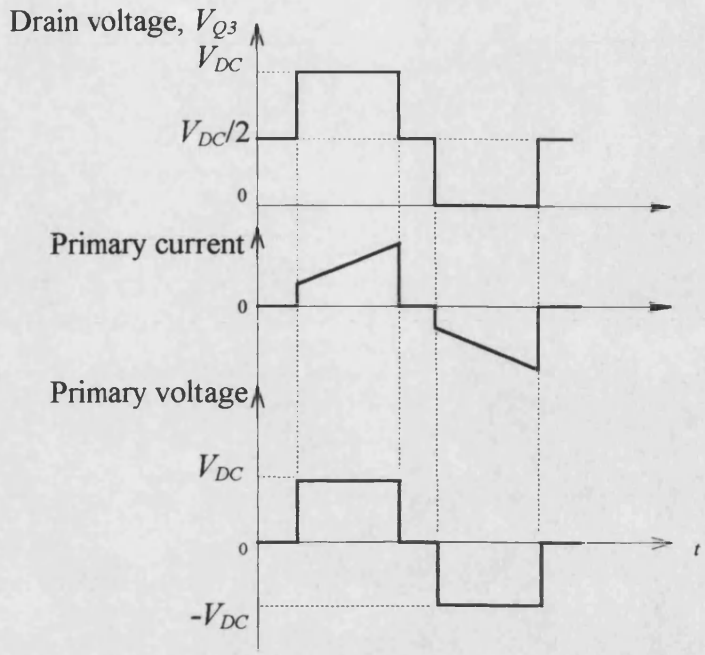


Fig. 2-17 Typical waveforms for a full-bridge converter

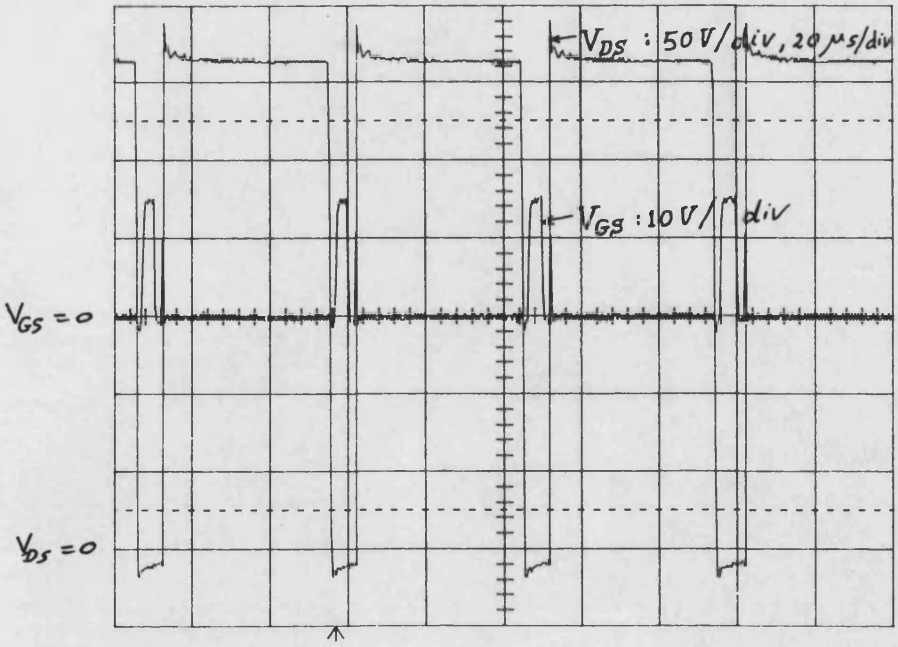


Fig. 2-18 Practical drain-source and gate-source voltages, V_{DS} and V_{GS}, for a full-bridge converter showing the effect of the magnetising and leakage inductance

FORWARD CONVERTERS

3-1 INTRODUCTION

Forward converters, unlike flyback ones, transfer or transform power to the load when the power switch is "on" and the power transformer in these converters is not used for storing energy.

In fact, the transformer-core flux, which builds up when the power is being transformed during the switch "on" period and represents stored energy, is now an embarrassment because it must be fully reset dissipatively or by circulating it through the converter input filter as quickly as possible during the switch "off" period. This is necessary to avoid reducing the maximum allowable switch "on" duty-cycle significantly.

In principle, therefore, dealing with this additional stored energy would seem to imply that forward converters are less efficient than flyback converters where all the stored energy may be transferred to the converter output. The forward converter, however, has other advantages which outweigh having to deal with the transformer reset energy, and for this reason it is used in various forms over a higher power range than the flyback converter.

This chapter describes three types of forward converters, namely:

1. Single-ended or one-transistor forward converters (also referred to as single-ended isolated forward converter [1]).

2. Double-ended or two-transistor forward converters (also referred to as diagonal half-bridge forward converters, or single-ended isolated hybrid bridge [1]).
3. Interleaved forward converters.

For each topology, the principle of operation and the main advantages and drawbacks are presented and briefly discussed. The effect of the reset winding turns on the peak primary current and the voltage stress is analyzed for single-ended forward converters, and illustrated by new graphs. A method of eliminating the main power device driving transformer from double-ended forward converters is also included, and interleaved forward converters are finally considered.

3-2 SINGLE-ENDED FORWARD CONVERTERS

The single-ended forward topology is the most widely used topology for converters of up to 200 W with an applied voltage range between 60 - 200 V.
The topology is very well documented in literature [1, 2, 3]. One of the main design problems is to optimize the utilization of the main power semiconductor switch. To facilitate this, a study on the effect of the number of reset winding turns on the peak primary current, and maximum voltage stress on the power switch is given here. However, to make it easier to understand this material, a brief description of the principle of operation of forward converters will first be presented.

3-2-1 Principle of Operation

Fig. 3-1 shows the power section of a single-ended forward converter which comprises a power transformer, TX_1, power switch, Q_1, clamping diode, D_1, rectifier diode, D_2, freewheeling diode, D_3, and output filter, LC. The transformer has three windings: a primary winding, N_P, secondary winding, N_S, and reset winding, N_R. It will initially be assumed that the primary and reset winding turns are equal.

When the power switch is turned "on", a magnetizing current is developed in the primary N_P, and the dot ends of all windings will be positive with respect to the other ends. The flux density, B, increases from the residual flux density, B_r, reaching the maximum working flux density, B_{MAX}, at the end of the "on" period. Diodes D_1 and D_3 become reverse-biased and cut off, while diode D_2 becomes forward-biased and conducts the full load current. Energy is added to the filter inductor, L, the capacitor, C, and the load R_L. Ignoring the voltage drop across Q_1 and the diodes, the voltage at point S will be:

$$V_S = V_{DC} \frac{N_S}{N_P} \tag{3-1}$$

Therefore, the power is delivered to the load during the "on" period of Q_1, from which the term *forward* is derived.

When Q_1 is turned "off", the energy stored in the magnetizing inductance reverses the polarities of all windings such that the dot ends become negative with respect to the other ends. D_2 will cut off, and D_1 conducts, thus clamping the voltage across N_R and N_P to V_{DC}. Therefore, the off-state voltage stress on the switch will be $2V_{DC}$. This stays for as long as energy remains in the magnetising inductance, at which time the voltage across all windings will be zero and the flux density returns back to B_r. Also during Q_1 turn-off, the energy stored in the filter inductor forces D_3 to conduct and pass the full load current.

Fig. 3-2 shows idealized waveforms for operation as previously described, where the spike on the drain of Q_1 at turn-off due to the primary leakage inductance has also been added.

3-2-2 Effect of Reset Winding Turns

In the above discussion, it was assumed that N_R=N_P. Therefore, the voltages across both windings are equal and, hence, the voltage stress on the power switch is twice the supply voltage plus some primary leakage inductance spike.

The number of turns used for the reset winding plays an important role in designing the forward converter as it determines, among other parameters, the peak current flowing in the primary, and the maximum reverse voltage stress which the switch should withstand.

At the end of the "on" pulse, the approximate primary winding volt-second integral is $T_{ON} \cdot V_{DC}$. To reset the core, a reverse volt-second integral must be applied to a winding to bring the core flux back to the starting point before the next "on" pulse starts. If this does not occur, the flux will increase slightly with each cycle, until the core eventually saturates, and Q_1 is destroyed by an excessive magnetising current.

If N_R is the same as N_P, then at turn off, a reverse voltage of approximately V_{DC} is induced across N_R and, hence, across N_P. Therefore, a time equal to T_{ON} is also required to reset the core, imposing a maximum limit on the "on" period of 50% of the switching period.

If N_R is less than N_P, then the voltage induced across N_P is higher than V_{DC}, and less time is required to reset the core. In this case, T_{ON} may be increased to more than 50% of the switching period, thus reducing the peak primary current for the same output power. But because the voltage induced across N_P in this case is higher than V_{DC}, the reverse voltage on the drain of Q_1 will be higher than $2V_{DC}$.

On the other hand, if N_R is greater than N_P, the voltage induced across N_P is lower than V_{DC}. This requires a longer time to reset the core. In this case, T_{ON} should be shorter, thus increasing the peak primary current for the same output power. Also, because the induced voltage across N_P is lower than V_{DC}, the reverse voltage on the drain of Q_1 is less than $2\ V_{DC}$.

Quantitatively, the effect of the reset winding turns can be evaluated as follows:

Let us assume that T_{ON} is the "on" period of the switch Q_1, T_R is the "reset" period of the core. $T_{ON} + T_R$ should be less than or equal to T_S, the total period of the operating cycle. Let us also define the factor:

$$\alpha = \frac{T_{ON} + T_R}{T_S} \qquad (3\text{-}2)$$

which is usually assumed 0.8, since some safety margin is always left. The flux excursion during the "on" period is:

$$\Delta\phi_{ON} = \frac{1}{N_P}\int v_P \, dt = \frac{V_{DC}T_{ON}}{N_P} \tag{3-3}$$

During the "off" period, the voltage across the reset windings is clamped at approximately V_{DC} by D_1. Therefore, the reverse flux excursion is:

$$\Delta\phi_{OFF} = \frac{1}{N_R}\int V_{DC} \, dt = \frac{V_{DC}T_R}{N_R} \tag{3-4}$$

For correct resetting, the following condition should be satisfied:

$$\Delta\phi_{ON} = \Delta\phi_{OFF} \Rightarrow T_R = \frac{N_R}{N_P} T_{ON} \tag{3-5}$$

This result has been reached elsewhere [3] but in a different analysis.
From Eq's (3-2) and (3-5), it can be written:

$$T_{ON} = \frac{\alpha \cdot T_S}{1 + N_R / N_P} \tag{3-6}$$

If η is the efficiency of the converter, and assuming L is large such that the amplitude of the current ramp, ΔI, is very small, then:

$$P_{IN} = \frac{P_O}{\eta} = V_{DC} \cdot I_{AV} = V_{DC} \cdot I_P \cdot \frac{T_{ON}}{T_S} \tag{3-7}$$

where: P_{IN} is the input power,

P_O is the output power,

I_{AV} is the average primary current,

I_P is the peak primary current.

Combining Eq's (3-6) and (3-7) gives:

$$I_P = \frac{1}{\alpha\eta}\frac{P_O}{V_{DC}}(1+\frac{N_R}{N_P}) \tag{3-8}$$

The maximum primary current, $I_{P(max)}$ occurs at minimum supply voltage, $V_{DC(min)}$, i.e.

$$I_{P(\max)} = \frac{1}{\alpha\eta}\frac{P_O}{V_{DC(\min)}}(1+\frac{N_R}{N_P}) \tag{3-9}$$

The maximum "off" voltage stress on Q_1 is:

$$V_{Q1(\max)} = V_{DC(\max)} + \frac{N_P}{N_R}V_{DC(\max)} = V_{DC(\max)}(1+\frac{N_P}{N_R}) \tag{3-10}$$

Fig. 3-3 shows how $I_{P(\max)}$, normalised to a base of $V_{DC(\min)} / P_O$, varies with the ratio N_R/N_P for different values of $\alpha\eta$. If $\alpha = 0.8$, $\eta = 0.8$, and N_R=N_P, then:

$$I_{P(\max)} = 3.12(\frac{P_O}{V_{DC(\min)}}) \tag{3-11}$$

Fig. 3-4 shows how $V_{R(\max)}$ varies with the ratio N_R/N_P. When this ratio is 1, $V_{R(\max)} = 2V_{DC(\max)}$. Also shown on the same figure, another curve for $V_{R(\max)}$ taking into consideration a leakage spike of 20% of the reverse voltage.

Fig's 3-3 and 3-4 can be used as a guide to simplify understanding the effect of the reset winding turns, and help in calculating N_R to suit the application. From these two figures, it can be seen that there is no point of increasing N_R more than 1.5 times N_P, as the current increases at a higher rate than the voltage decreases, unless the maximum voltage is high and/or the maximum current is low. Below N_R/N_P=0.5, the reverse voltage increases considerably. Therefore, it is not recommended to work in this area.

A more generalized graph showing the effect of the ratio of reset winding turns to primary winding turns, ζ, on the switched volt-ampere, VA, can be obtained by multiplying Eq's (3-9) and (3-10) and dividing it by P_O, to give:

$$(VA)_n = \frac{I_{P(max)} V_{Q(max)}}{P_O} = \frac{\frac{1}{\alpha\eta}\frac{P_O}{V_{DC(min)}}(1+\zeta)\cdot V_{DC(max)}(1+\frac{1}{\zeta})}{P_O}$$

$$= \frac{1}{\alpha\eta}\frac{V_{DC(max)}}{V_{DC(min)}}(1+\zeta)(1+\frac{1}{\zeta}) \qquad (3\text{-}12)$$

where:

$$\zeta = \frac{N_R}{N_P} \qquad (3\text{-}13)$$

If the range of the d.c. supply voltage is small, i.e. $V_{DC(max)} \approx V_{DC(min)}$, Fig. 3-5 can be obtained for different values of $\alpha\eta$.

Since the power switch cost is related to the switched VA which determines the silicon area of the required switch, then Fig. 3-5 may be used to indicate how the power switch cost changes with the ratio N_R/N_P. It is clearly seen that the optimum ratio is one, i.e. $N_R = N_P$, which gives the lowest power switch cost.

3-2-3 Effect of Leakage Inductance in Single-Ended Forward Converters

Single-ended forward converters, as has been shown, incorporate a power transformer that has three windings, each of which may have its own leakage inductance, as shown in Fig. 3-6, where L_{LKP}, L_{LKR} and L_{LKS} are the leakage inductance of the primary, reset and secondary windings, respectively. In addition to these, stray inductance, L_{STRAY}, may also exist due to external connections between components.

During Q turn-on, energy has been stored in L_{STRAY}, L_P and L_{LKP}. At Q turn-off, a reverse voltage is generated across each of which and may be calculated as follows, assuming $N_R = N_P$:

$$V_1 = L_{STRAY}\frac{di_P}{dt} \tag{3-14}$$

$$V_2 = V_4 = V_{D1} + V_{DC} + V_1 \tag{3-15}$$

$$V_3 = L_{LKP}\frac{di_P}{dt} \tag{3-16}$$

Therefore, the worst-case spike at Q drain can be calculated as:

$$\begin{aligned} V_{SPIKE} &= V_1 + V_2 + V_3 + V_{DC} \\ &= 2V_{DC} + V_{D1} + (2L_{STRAY} + L_{LKP})\frac{di_P}{dt} \end{aligned} \tag{3-17}$$

which shows that L_{STRAY} has a double effect on the voltage spike.

On the other hand, L_{LKR} has no effect on the voltage spike, as the current through it at turn-off is zero. L_{LKS} also has no effect on the spike level and only reduces the voltage stress on the rectifier diode D_2 at turn-off [4].

3-2-4 Advantages of Single-Ended Forward Converters

1. Single-ended forward converters use only one quadrant of the hysteresis loop. Therefore, they do not suffer from the shortcoming of flux imbalance usually encountered in push-pull circuits, which simplifies their design and increases reliability.
2. Compared to push-pull circuits, single-ended forward converters incorporate one transistor and associated driver and heatsink. Therefore, they are more economical in cost and required space.
3. Compared to flyback converters, they have less current and voltage ripple in the output circuit. Therefore, the ripple current rating of the filter capacitor is lower [2].
4. Because of (3) above, the peak primary current is less [2], which reduces the generated EMI.

3-2-5 Disadvantages of Single-Ended Forward Converters

Although single-ended forward converters have several advantages over other converters, they suffer from some drawbacks due to their operating principle. These include the following:

1. They require an additional reset winding and associated fast-recovery diode, which increases the cost of the converter.
2. The maximum duty-cycle is 50%, if N_R=N_P. Therefore, the peak primary and secondary currents are higher compared to push-pull circuits. This generates higher EMI and causes higher power loss.

Compared to flyback converters:

3. They require an output filter inductor and freewheeling diode, which increases the complexity of the circuit and its cost.

3-3 DOUBLE-ENDED FORWARD CONVERTERS

3-3-1 Introduction

As described in the previous section, the power transistor in single-ended forward converters may be subjected to twice the supply voltage, plus some leakage spike due to the leakage inductance. Therefore, single-ended forward converters are uneconomic when operating directly from (220 to 240) Vrms a.c. supplies. Double-ended forward converters, on the other hand, employ two transistors and two diodes connected in such a way that each transistor is subjected to only the supply voltage. Furthermore, the transformer leakage inductance has no effect in this type of converters since the peak voltage generated is clamped by the diodes to about V_{DC}, as later shown.

3-3-2 Principle of Operation

Fig. 3-7 shows the power stage of a double-ended forward converter. At the start of the "on" pulse, both power switches Q_1 and Q_2 are turned "on" by the control circuit. The primary is subjected to approximately the full supply voltage V_{DC}, and power is delivered to the load during this period as in single-ended forward converters, while diodes D_1 and D_2 are cut off. At the end of the "on" pulse, both switches are turned "off" simultaneously. The energy stored in the magnetizing inductance reverses the voltage polarity on all windings. The voltage at the source of Q_1 will be limited by D_1 to one diode drop below ground, while the drain of Q_2 will be limited by D_2 to one diode drop above V_{DC}. D_1 and D_2 also clamp the leakage inductance spike. Therefore, both switches are subjected to only one diode drop above V_{DC} during turn-off, which is the main advantage of these converters over single-ended ones. Fig. 3-8 shows idealized typical waveforms for the double-ended forward converter.

3-3-3 Eliminating the Drive Transformer from Double-Ended Forward Converters

The power switch Q_1 in Fig. 3-7 requires a floating driving circuit as its source is not connected to ground. Usually, this is accomplished by incorporating a small driving transformer in the driver circuit, which is the major drawback in this type of converter. This drawback may be eliminated if the power switch used in the converter is a MOSFET, as will be described in the next paragraph.

MOSFET's are voltage controlled devices and need virtually no current throughout the "on" time. The drain current is turned "on" by a positive gate-to-source voltage (in an n-channel MOSFET), and does not flow until this voltage reaches a threshold level which differs from one transistor to another. The only current required from the driving circuit, is to charge the input capacitance, C_{ioss}, of the MOSFET. As soon as this capacitance has been charged to the threshold value, V_{TH}, current starts to flow in the MOSFET. When the charge action completes, virtually no further current is

needed. Fortunately, C_{ioss} of MOSFET's is not very large; it is in the order of a few nano-farads.

If an external charged capacitor with sufficiently large value is connected between the gate and the source of an "off" MOSFET instead of a driving source, some charge will be transferred to its input capacitance. This will slightly reduce the voltage across the external capacitor, but will still be large enough to keep the MOSFET "on". Some MOSFET driver IC's exist which exploit this feature, and are used for half- and full-bridge converters. Fig. 3-9 shows that a small driver transformer is not needed in these converters when using such IC's. The data sheet of such MOSFET driver is shown in App. (3-1).

The circuit shown in Fig. 3-9, works well for half- and full-bridge converters, where the source of the floating switch is the drain of the grounded one, and C_{ext} can charge through the "on" resistance of Q_2 when it is "on" and Q_1 is "off". In double-ended forward converters, where the primary of the transformer is connected between the first source and the second drain, then this circuit may not work.

It has been suggested [5] that a control IC, as shown in Fig. 3-10, can be used to drive the two MOSFET's with the addition of three components R_1, Q_3 and Q_4, where Q_3 is a high voltage MOSFET.

A closer examination of a double-ended forward converter (see Fig's 3-7 and 3-8) during steady-state operations, shows that during the turn-off, the voltage at the no-dot end of the primary, V_B, is at one diode drop above V_{DC}, while the voltage at the dot end, V_A, is at one diode drop below ground. This means that if C_{ext} is connected to point A, as shown in Fig. 3-11, it will charge during the "off" period of both switches through the transformer for as long as energy remains in the magnetising inductance. It does not charge through the "on" resistance of Q_2, as was the case in Fig. 3-9.

Analysis of the circuit of Fig. 3-11, which is rearranged in Fig. 3-12, shows that during the turn-off, the magnetising inductance, L_M, resets against V_{DC}. However, if V_{Cext} is less than V_{CC}, the transformer magnetising current will flow in both D_5 and D_1. Once C_{ext} is charged slightly above V_{CC}, D_5 is cut off and i_M flows virtually fully in D_1. On the other hand, C_{ext} charging current flows in the components N_P, D_2, V_{DC}, V_{CC},

D_5 and C_{ext}, and is a part of the magnetising current. The voltage developed across C_{ext} will be used as a floating supply to drive Q_1, as will be shown in a moment.

A question arising is, what happens at start-up when C_{ext} is discharged and no voltage is available to turn Q_1 "on". In this case, no current flows in the primary, since both switches should be "on" simultaneously in this type of converters. This means that the source of Q_1 will not be at one diode drop below ground, because the circuit has not started yet, and C_{ext} will not charge; Q_1 will never turn "on" and the circuit will never start.

Examination of the circuit shown in Fig. 3-11 shows that even when Q_1 is "off", when Q_2 is "on", a current flows from V_{CC} to D_5 and C_{ext}, through the primary of TX_1, completing its path to ground through the on-resistance of Q_2. This current charges C_{ext} slowly, and a voltage will build up across C_{ext}, until it reaches the voltage level required by the driving IC ($\approx$8.5 V). Once this voltage is reached, both pulses from the driving IC will now drive the switches and the circuit starts working normally. The circuit shown in Fig. 3-11 was simulated in PSPICE, and the voltage across C_{ext} was recorded to be as shown in Fig. 3-13. Therefore, it seems that the control IC can be used to drive the double-ended forward converter without the addition of extra components, and can be self-started. The value of the bootstrap capacitor can be calculated as described in App. (3-2).

3-3-4 The Practical Circuit

A double-ended forward converter, as shown in Fig. 3-14, is built without employing a driver circuit transformer to verify the previous analysis. The specifications of the circuit are as follows:

Input voltage range, $V_{IN} = (170-350)$ V d.c. from 120 or 240 V a.c. system.

Output voltage, $V_O = 12$ V d.c.

Load current, $I_L = 10$ A

Switching frequency, $f_{SW} = 50$ kHz.

3-3-4-1 Transformer design

The available core in the lab is EC70/34/17, type FX3750 from Mullard which has the following specifications:

- Core material is 3C8
- Effective cross-sectional area, $A_e = 279\ \text{mm}^2$
- Saturation flux density, $B_S = 350\ \text{mT}$ @100°C

It will be assumed that the maximum working flux density, B is 300 mT to ensure that the core does not saturate under transient conditions. The flux density should be obtained at the maximum input voltage of 350 V. If the maximum duty-cycle is 50%, i.e. $T_{ON} = 10\mu s$, the number of primary turns can be calculated as:

$$N_P = \frac{V_{DC(\max)} T_{ON(\max)}}{BA_e} = \frac{350 \times 10 \times 10^{-6}}{0.3 \times 279 \times 10^{-6}} \approx 41.8$$

This will be assumed to be 42 turns.

The secondary voltage will be calculated from the required d.c. output voltage as:

$$V_S = \frac{V_O(T_{ON} + T_{OFF})}{T_{ON}} + V_D = \frac{12(10+10)}{10} + 1 = 25\ \text{V}$$

where V_D is the voltage drop across the rectifier, which is assumed 1 V.

The minimum primary voltage which should give the above V_S is:

$$V_{P(\min)} = V_{DC(\min)} - 2V_{DS(on)} = 170 - 4 = 166\ \text{V}$$

where it is assumed that the voltage drop across each power switch is 2 V when it is "on". Now number of secondary turns can be calculated:

$$N_S = \frac{N_P V_S}{V_{P(\min)}} = \frac{42 \times 25}{166} = 6.3$$

This will be assumed to be 7 turns.

A gap of 0.1 mm will be used to reduce the effect of saturation.

Primary wire diameter = 1.3 mm, and secondary wire diameter = 2 mm.

3-3-4-2 Practical considerations

To obtain the best performance from the converter, diodes D_1 and D_2 should be as close as possible to the power switches. The leads of the input storage capacitor should be twisted, and the capacitor should be very close to the switches. At first, the length of these leads were 35 cm each and not twisted. The resulted spike on the drain was 80 V. When the leads are twisted and their length reduced to 8 cm, the voltage spike reduced to 25 V at maximum input voltage. Therefore, in this type of converter, and because of the clamping diodes, the leakage inductance of the transformer has no effect if the above is taken into consideration, and there is no need for snubber capacitors, which is a big advantage in these converters.

3-3-4-3 The effect of input voltage, load current and switching frequency

The circuit has been designed to give 12 V d.c. with an input voltage of 170 V d.c. derived from a 120 V a.c. supply, and maximum duty-cycle of 50%. Table 3-1 shows how T_{ON} changes with the input voltage, where the shortest "on" period is 4.9 μs at maximum input voltage. The circuit works normally, and the bootstrap capacitor is fully charged each cycle. The "on" period was deliberately decreased to 2 μs and the circuit still worked normally, although it was not designed to work at these short periods.

a.c. voltage (V)	d.c. voltage (V)	T_{ON} (μs)	output voltage (V)	output current (A)
120	170	10	12	10
235	330	4.9	12	10

Table 3-1 Changes of the "on" period with input voltage

Below 2 μs, the circuit fails to function properly, as this period is not enough to charge the bootstrap capacitor to the required value.

In the input voltage range of interest, the load current has been changed from the no-load to full-load with normal circuit operation.

The switching frequency has been increased to 200 kHz without any problem. Above 200 kHz, the minimum available "on" period is not enough to fully charge the bootstrap capacitor to the required value, and the circuit fails to work properly.

3-3-4-4 Practical waveforms

Fig. 3-15 shows the drain-source voltage of the lower MOSFET and the source voltage of the upper one, at maximum and minimum input voltages, and no- and full-load current.

3-3-5 Advantages of Double-Ended Forward Converters

1. Power switches are subjected to only one diode drop above the supply voltage V_{DC}.
2. Leakage inductance has no effect on increasing the voltage stress on power switches due to clamping diodes, and the energy stored in the magnetizing inductance is returned to the d.c. link filter capacitor.
3. The energy recovery winding is not required.

3-3-6 Disadvantages of Double-Ended Forward Converters

1. Using two power switches increases the cost of the converter and the requirement of assembly and increases power loss.
2. Isolated drive is required if bipolar transistors are used, because of the added power switch.
3. Two fast action clamping diodes are required.
4. The maximum duty-cycle is 50%, which means high peak currents and, hence, high power loss and EMI.

3-4 INTERLEAVED FORWARD CONVERTERS

3-4-1 Principle of Operation

The interleaved forward converter, as shown in Fig. 3-16, comprises two identical single-ended forward converters which operate on alternate half cycles. The secondary currents from both converters are added to form the load current. Therefore, for the same output power, the primary current in each converter is half that of a single-ended forward converter.

3-4-2 Advantages of Interleaved Forward Converters

1. Since the EMI is proportional to the peak current, interleaved forward converters generate less EMI compared to single-ended ones supplying the same output power [2].
2. Two transistors used in an interleaved forward converter, may be less expensive than a single one used in a single-ended forward converter having twice the current ratings.
3. Compared to a single-ended forward converter supplying the same output power, the secondary diodes in an interleaved forward converter are subjected to half the reverse voltage of that in the former. This is particularly useful at high output voltages since, with lower reverse voltage, diodes have shorter reverse-recovery time; accordingly less power is dissipated by secondary diodes.

3-4-3 Disadvantages of Interleaved Forward Converters

Compared to push-pull converters, interleaved forward converters are most likely to be more expensive, and occupy more space. This might be balanced by the fact that in interleaved forward converters there is no flux imbalance problem which might occur in push-pull converters under some transient conditions.

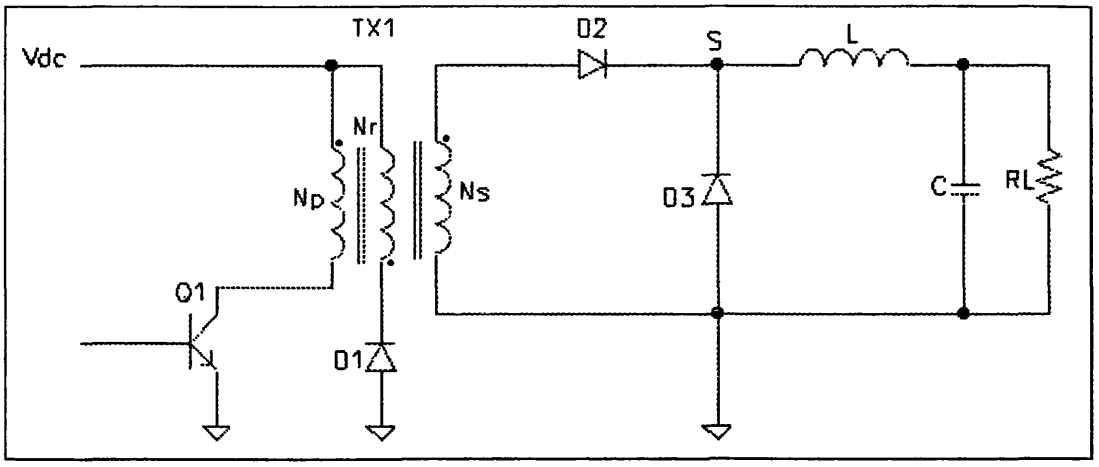


Fig 3-1 Single-ended forward converter

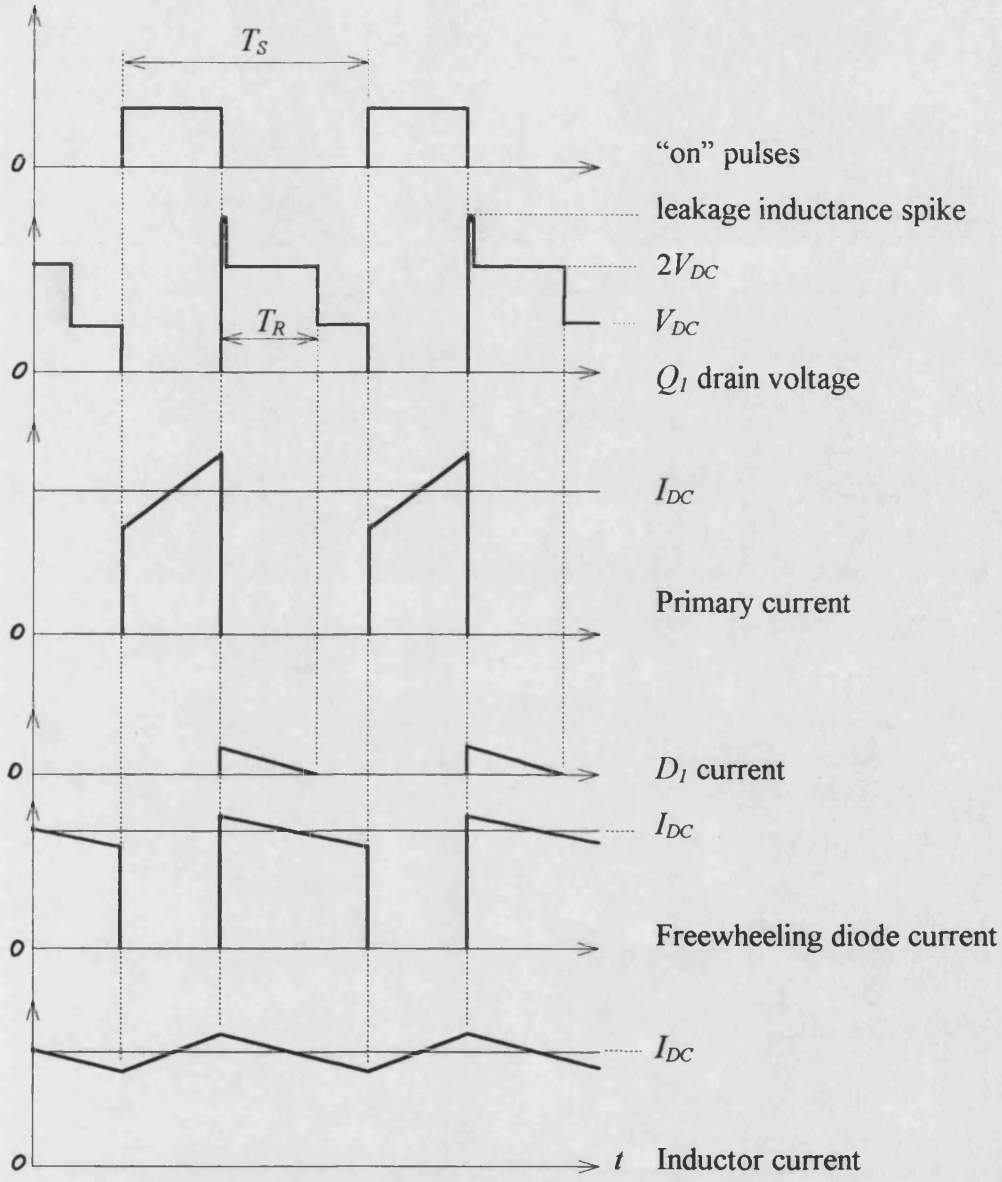


Fig. 3-2 Typical waveforms of single-ended forward converter (T_R = Transformer reset period)

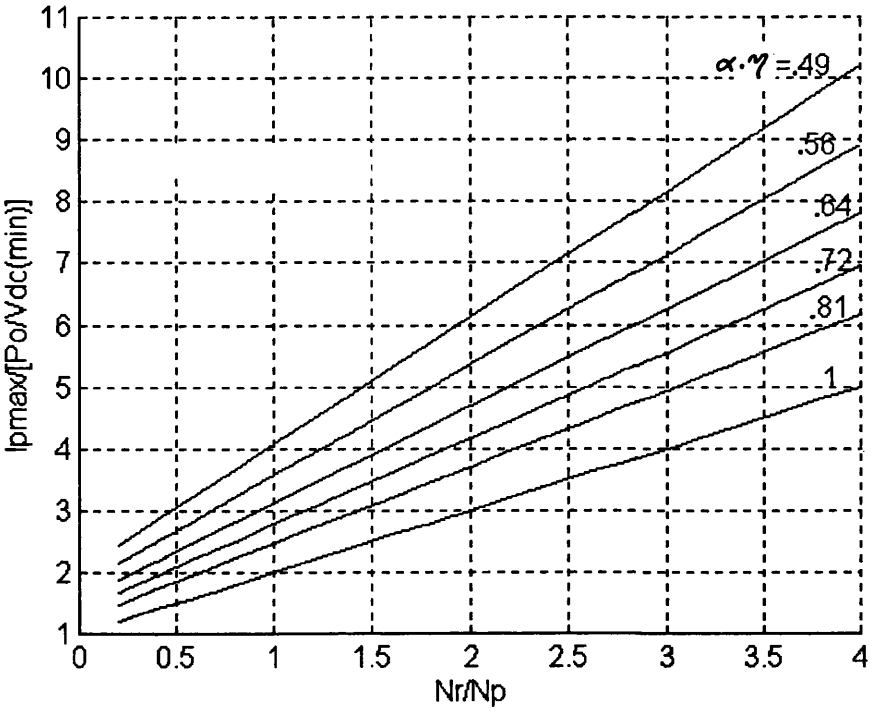


Fig. 3-3 Normalised $I_{P\max}$ as a function of N_R/N_P for different values of $\alpha\eta$

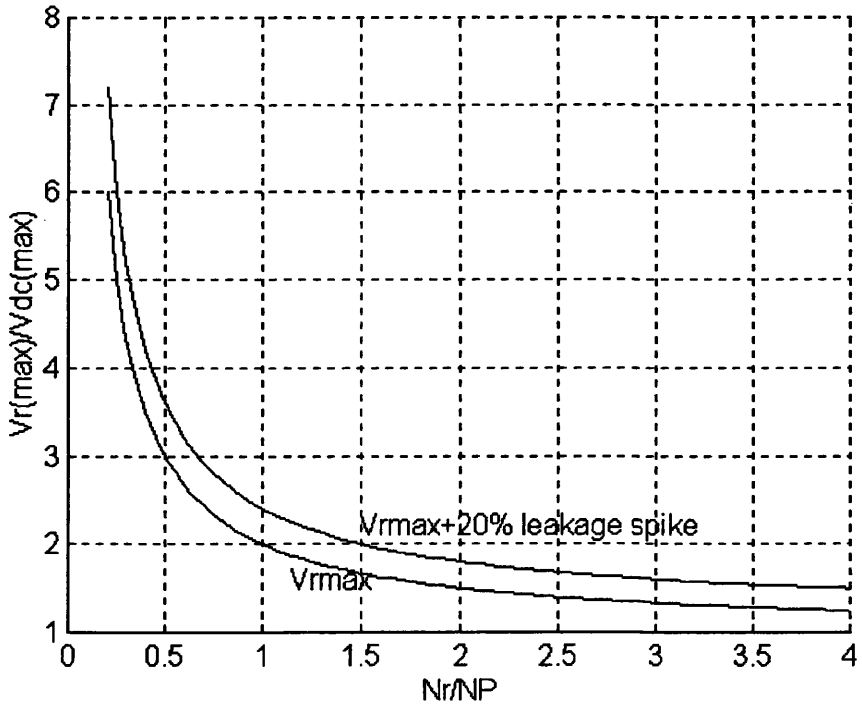


Fig. 3-4 Normalised $V_{R\max}$ as a function of N_R/N_P

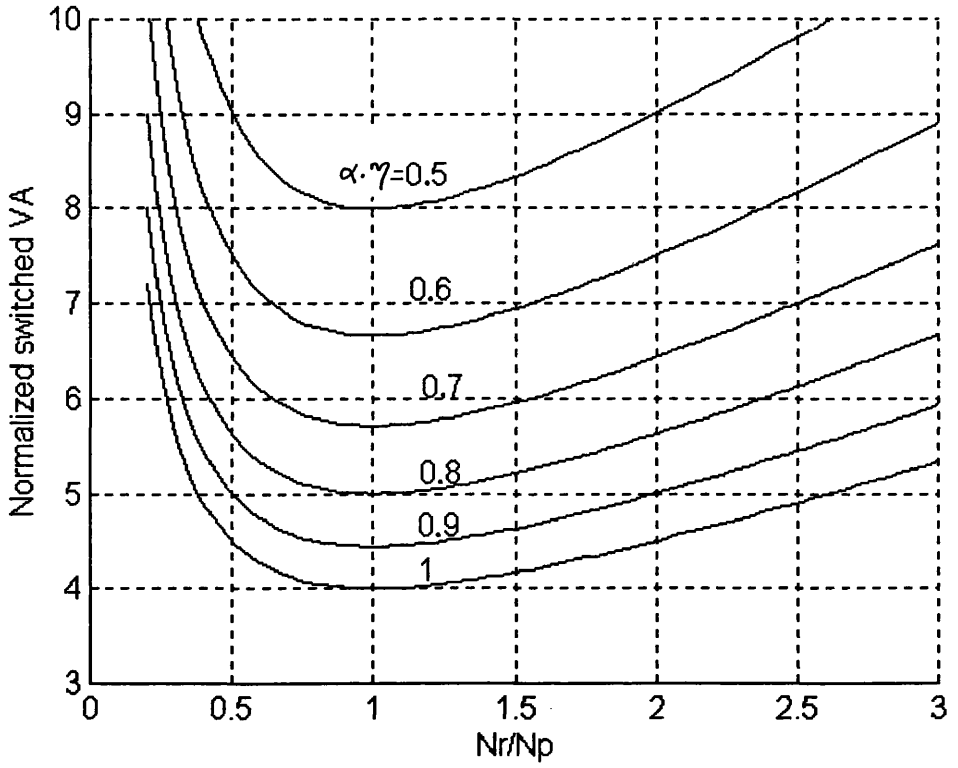


Fig. 3-5 Normalised switched VA versus N_R/N_P for different values of $\alpha\eta$

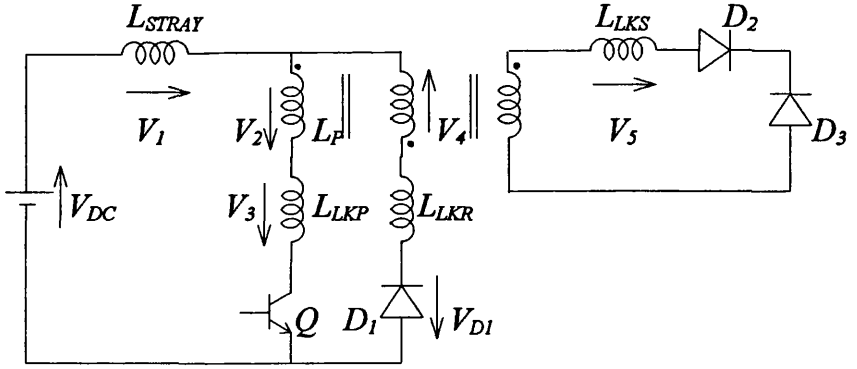


Fig. 3-6 Single-ended forward converter showing possible leakage and stray inductance together with voltage polarities at turn-off

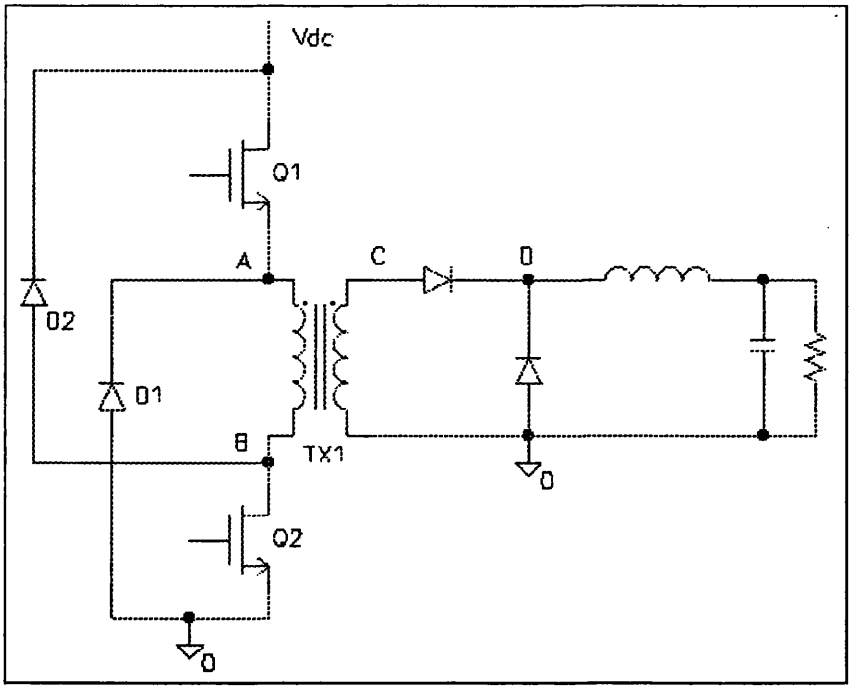


Fig. 3-7 The power section of a double-ended forward converter

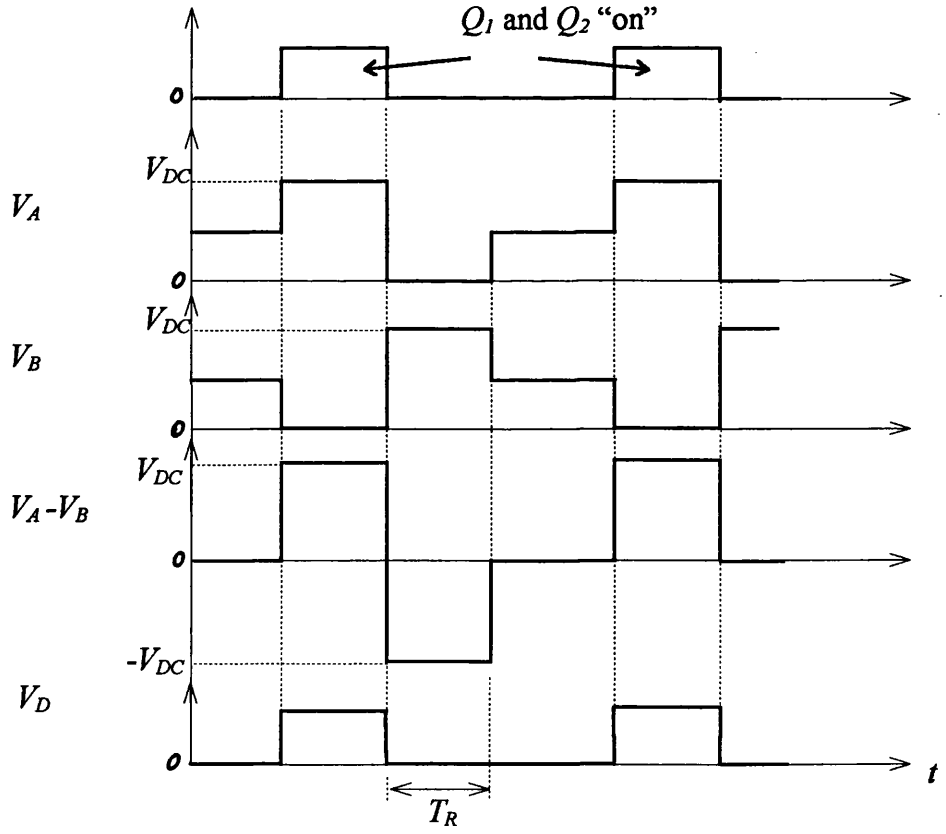


Fig. 3-8 Different typical waveforms for double-ended forward converters
(T_R = transformer reset period)

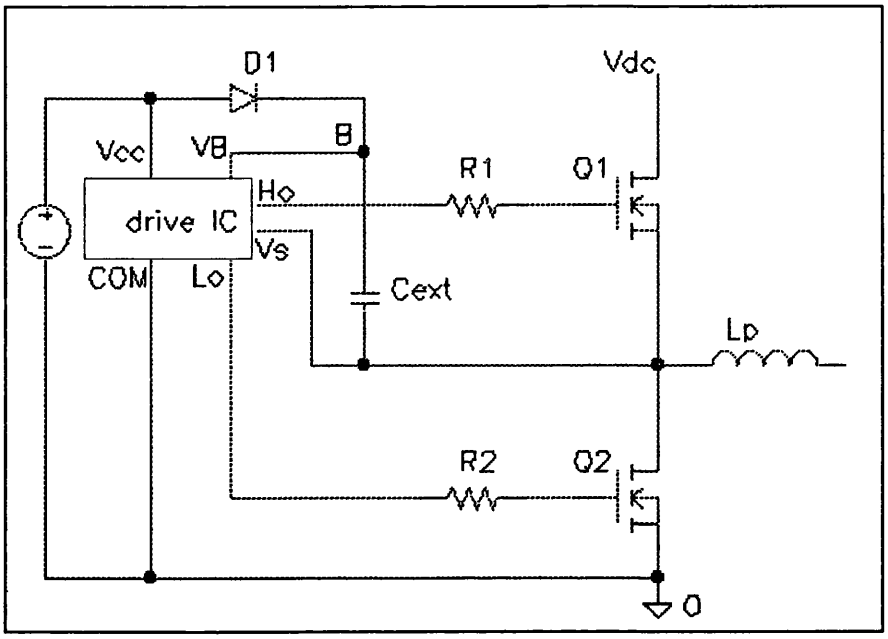


Fig. 3-9 A MOSFET driver for floating switches

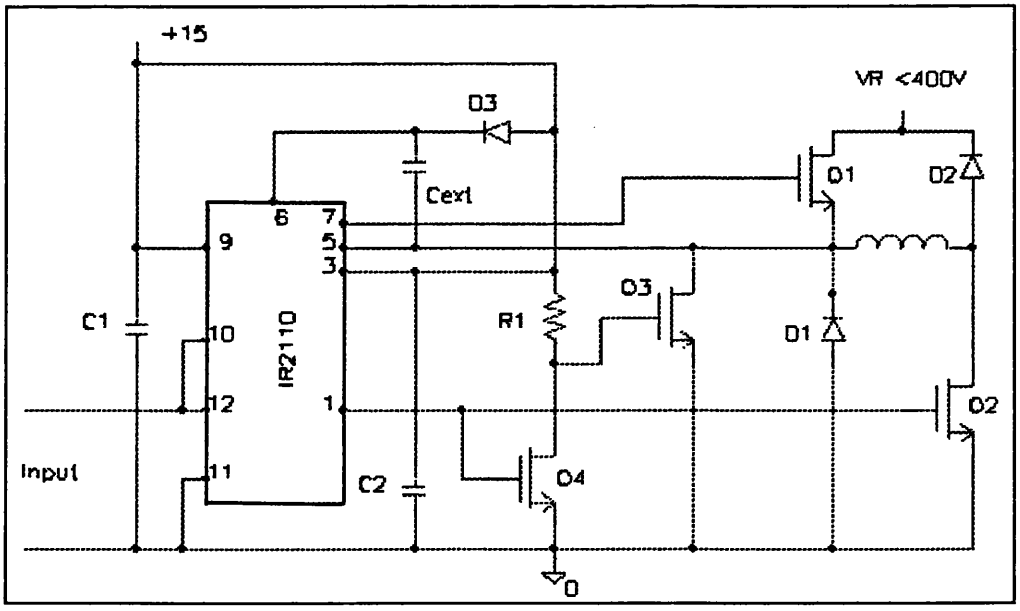


Fig. 3-10 Controlling a double-ended forward converter by a control IC [5]

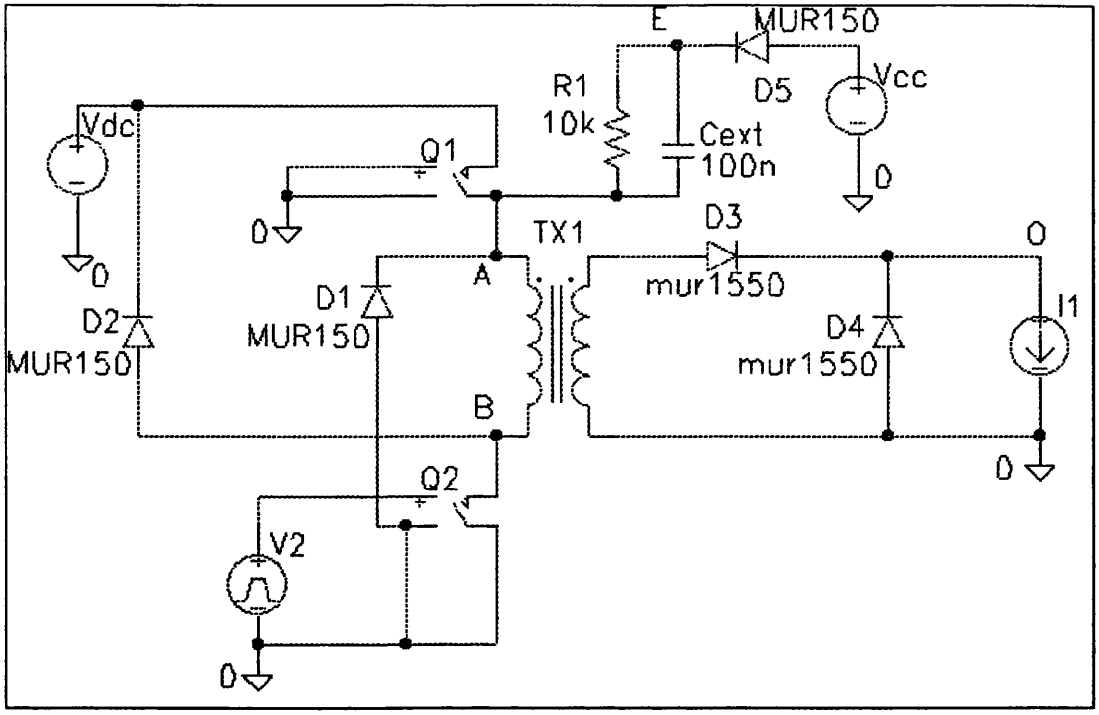


Fig. 3-11 The circuit used to simulate a double-ended forward converter to show that C_{ext} can fully charge during the start-up

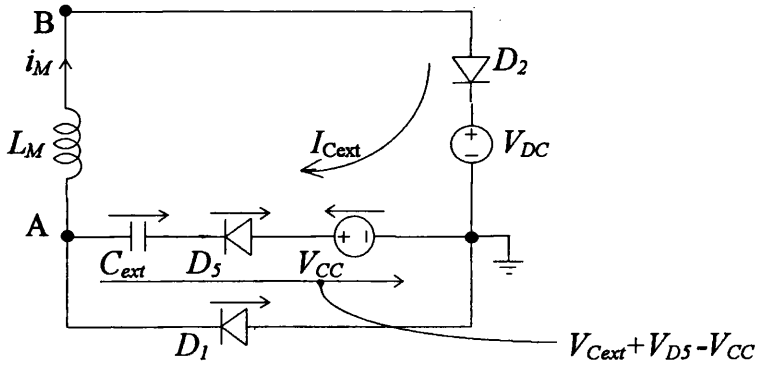


Fig. 3-12 Rearrangement of the circuit of Fig. 3-11 showing the recovery and C_{ext} charging current paths

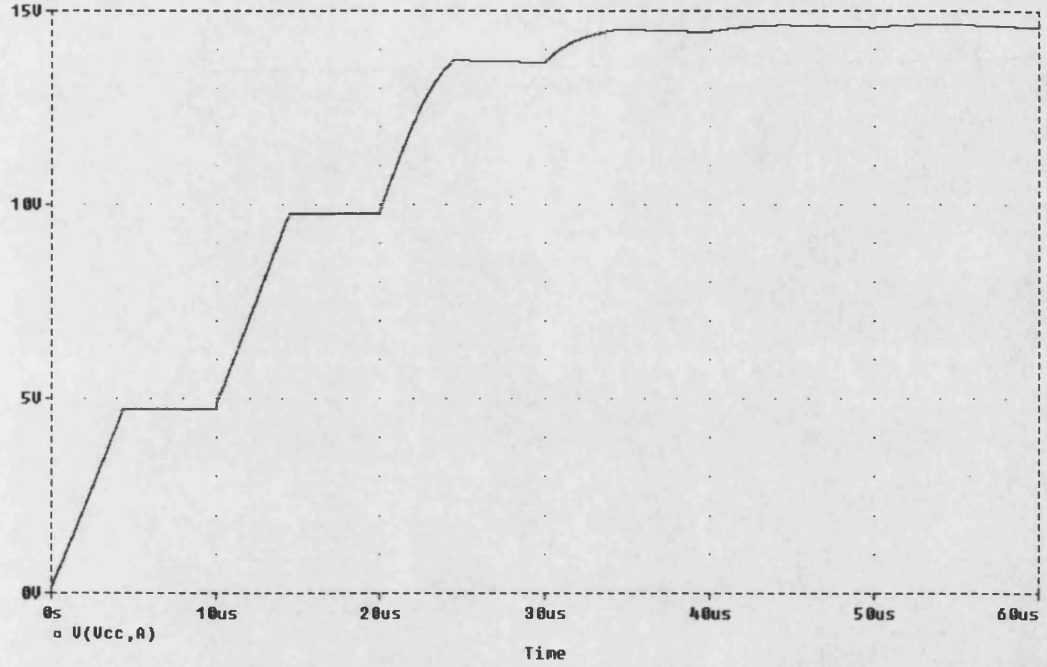


Fig. 3-13 The start-up voltage across C_{ext} as simulated in PSPICE

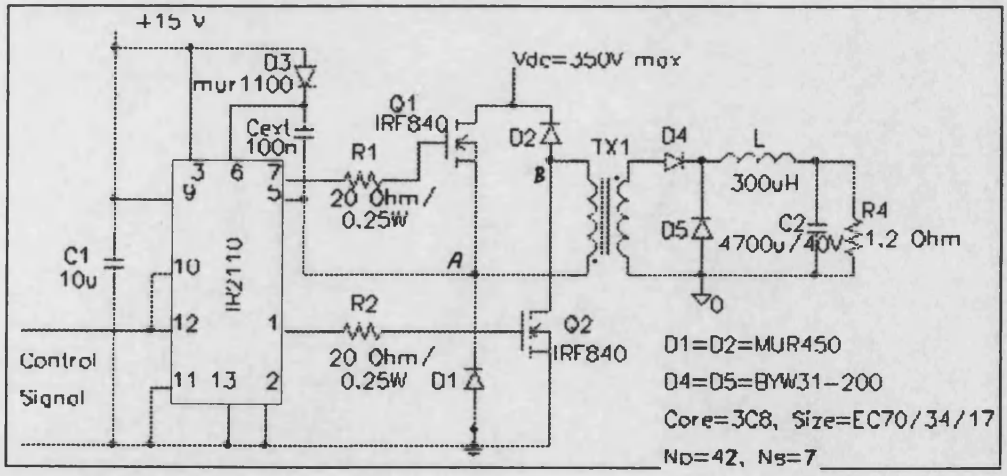
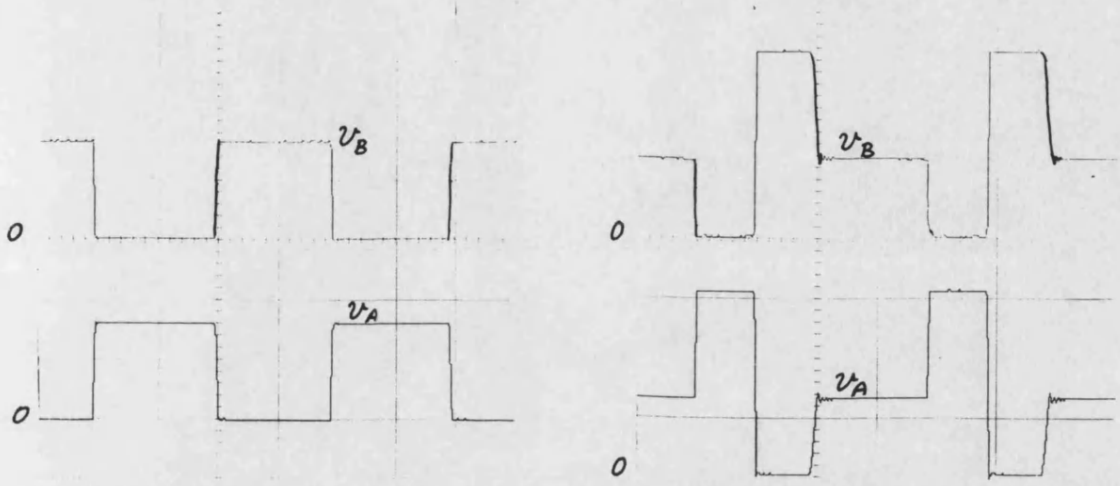
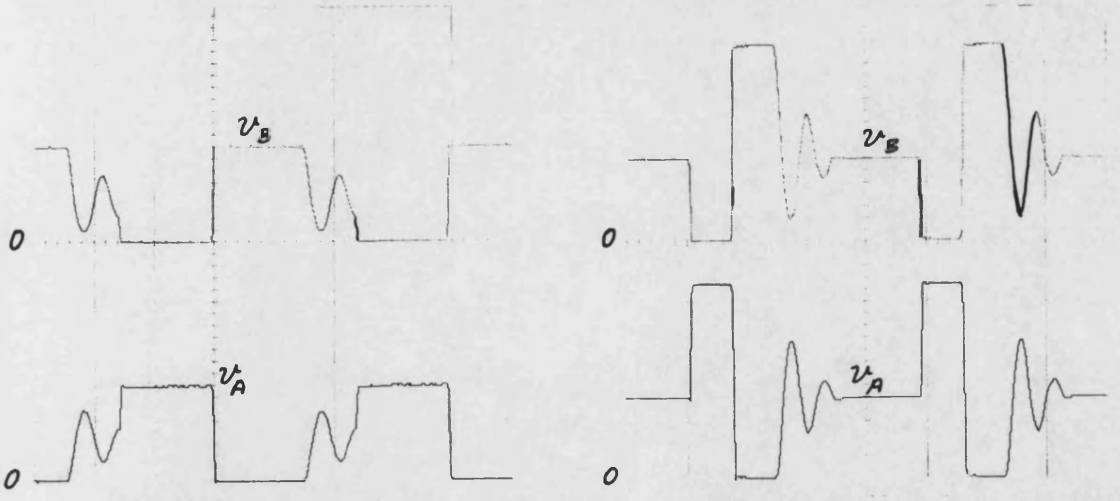


Fig. 3-14 Practical double-ended forward converter employing a control IC instead of a small driver transformer



a) V_{IN} = 170 V d.c., I_L = 10 A

b) V_{IN} = 330 V d.c., I_L = 10 A



c) V_{IN} = 170 V d.c., I_L = 0 A

d) V_{IN} = 330 V d.c., I_L = 0 A

Fig. 3-15 Practical waveforms for the designed double-ended forward converter
100V/div, 10μs/div

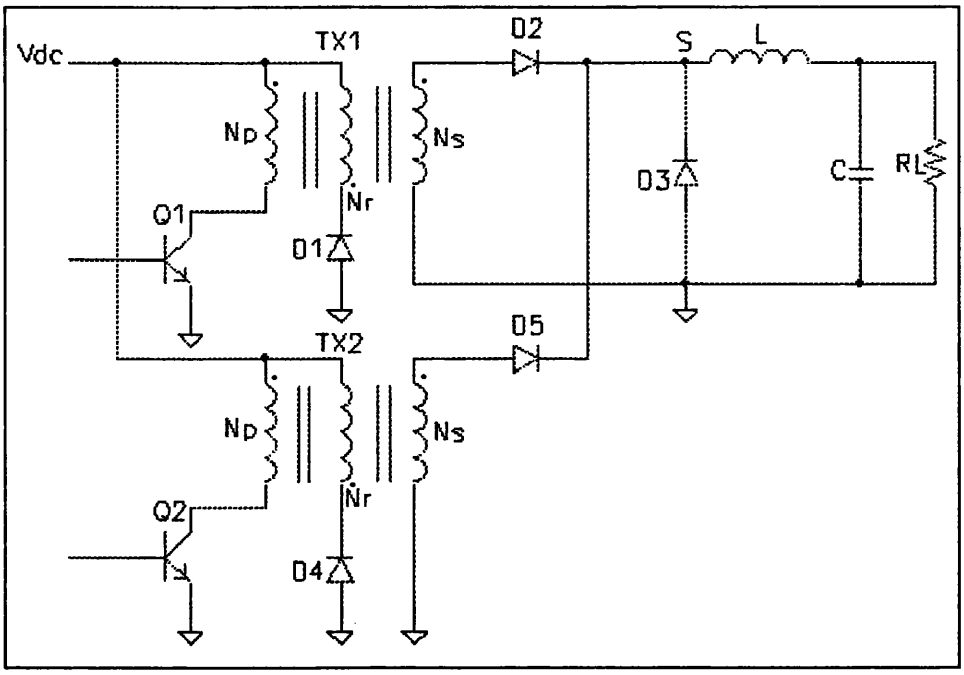


Fig. 3-16 The power section of an interleaved forward converter

CHAPTER THREE REFERENCES

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FLUX IMBALANCE IN PUSH-PULL CONVERTERS

4-1 INTRODUCTION

Transformer-isolated push-pull circuits are very widely used in dc/dc converters and dc/ac inverters at the low to medium power level. They suffer from several drawbacks, as described in Ch. 2. However, one of the biggest design challenges with them is preventing the possibility of transformer-core saturation which is likely to arise due to asymmetry in transformer centre-tapped windings or asymmetry in transformer-waveform excursions. Either effect produces asymmetric transformer-core flux excursions. Hence, the transformer core is not perfectly reset at the end of each switching cycle and the maximum working flux density in one direction is different from that in the other, as shown in Fig. 4-1b.

In an ideal circuit, the volt-second integrals of the primary-winding voltage-waveform of alternate half-cycles are equal. Therefore, the maximum working flux density, $+B_W$, will be equal (but of course in the opposite direction) to the minimum working flux density, $-B_W$, such that the working transformer-core hysteresis loop is symmetrical around the B/H axes origin, as shown in Fig. 4-1a.

For many reasons, the effective volt-second integral during one half-cycle may differ from that during the next half-cycle. The resulting flux imbalance accumulates over several cycles and the hysteresis loop moves up or down, depending on which direction has the larger volt-second integral. Eventually, the core saturates in that

direction. This saturation effect is also known as "staircase saturation", as the position of the hysteresis loop moves in steps into saturation each cycle.

Once the core saturates, the primary impedance decreases drastically, and a high current flows in the circuit limited only by the small primary-winding and source impedances. The destruction of the main power transistors is virtually certain if the primary current is not limited.

Although flux imbalance does not occur in properly-designed converters that use cores in one quadrant of the hysteresis loop, such as forward and flyback topologies and their derivatives, for equivalent power handling capability such converters generally achieve a lower transformer, filter capacitor and power-semiconductor device utilisation. This is due to higher current ripple in these than in better transformer-isolated converters, such as push-pull, half-bridge and full-bridge ones.

Also flux imbalance does not occur in the converter inductors found in un-isolated dc/dc converters such as buck, boost, buck-boost and polarity inverting converters. However, with these the benefits of transformer isolation is lost. It is worthwhile, therefore, to consider methods of eliminating the flux imbalance problem in push-pull converters.

4-2 FLUX IMBALANCE DESCRIPTION

The consequence of flux imbalance is best illustrated using a push-pull converter as shown in Fig. 4-2. In this, let us assume that the core operating point is at $-B_W$ (see Fig. 4-1a) at the instant when Q_1 is turned "on". Once Q_1 is turned "on", a voltage V_{DC} is applied to the primary P_1 (assuming lossless components), causing the flux density to move, say, up the hysteresis loop. This condition stays until the end of the "on" period of Q_1 at which time the operation point of the flux density will be at $+B_W$, as shown in Fig. 4-1a, making an excursion of $2B_W$. The amount by which the flux changes, depends on the area of the voltage waveform excursion applied to the primary P_1, i.e. the volt-second integral. During this period, D_1 conducts while D_2 is

subjected to a reverse voltage and is kept "off". At the end of the "on" period of Q_1, both switches are set "off". During this period, which is called the dead time, all voltages across primaries and secondaries will virtually be zero, and hence there is very little change in the flux (see Ch. 2 for more details on this).

At the end of the dead time, Q_2 is turned "on" and the same voltage V_{DC} is applied to P_2. The flux density moves down the hysteresis loop by the same amount such that at the end of the conduction period, the operating point lies exactly at $-B_W$ making an excursion of $2B_W$. At the end of this "on" period both switches are "off" and there is no change until Q_1 is turned "on" again and the cycle repeats, and the flux density waveform will be as shown in Fig. 4-1a.

This condition thus described will stay as long as the volt-second integral during the first "on" time equals that during the second "on" time, and the flux transition will be symmetrical around zero.

If the volt-second integral during, say, the first "on" time is higher than that during the second "on" time as shown in Fig. 4-3a, the maximum flux density operating point moves each cycle by some amount depending on the inequality of the volt-second integral, and the hysteresis loop moves up slowly as shown in Fig. 4-3b until it reaches saturation.

4-3 REASONS OF FLUX IMBALANCE

The magnetic flux in a core is given, according to Faraday's Law, by :

$$\phi = \frac{1}{N_P}\int V_P \, dt \qquad (4\text{-}1)$$

In dc/dc converters, the voltage V_P is approximately constant, and therefore Eq. (4-1) can be rewritten as:

$$\phi = \frac{1}{N_P} V_P \, T_{ON} \tag{4-2}$$

where N_P is the number of turns of the winding at which the voltage V_P is applied, T_{ON} is the "on" period defined by the control circuit and other factors as will be seen shortly, and V_P is the d.c. voltage minus the voltage drop across the power switch when it is "on", i.e.

$$V_P = V_{DC} - V_{ON} \tag{4-3}$$

Any mismatch in any of the above parameters during each half-cycle may lead to flux imbalance and, as a consequence, to saturation.

The following describes the effect of the parameters in Eq's (4-2) and (4-3) on the flux imbalance, in addition to some other factors that also have their own effects.

4-3-1 Turn-on time, T_{ON}

T_{ON} is defined as the period that starts when one switch is turned "on", until the same switch is turned off. This period is mainly determined by the control circuit to keep the output voltage within a certain limit, and any mismatch within the control circuit, or the response of the feedback loop to the output-voltage or load-current variations, may lead to mismatch in the output "on" pulse from the control circuit. In addition, if bipolar transistors are used, there is always a storage time required to remove the excess charge from the base before the transistor can be turned off. This parameter has wide production spread and is temperature-dependant. So it is not unusual to have different storage times and, therefore, different T_{ON} times.

4-3-2 Primary voltage, V_P

Eq. (4-3) shows that V_P depends on V_{DC}, the d.c. supply voltage, and the on-state voltage of the power switch. V_{DC} is usually assumed constant, although some ripple may exist riding on this voltage. V_{ON} ($V_{CE(sat)}$ for bipolars, or $V_{DS(on)}$ for MOSFET's)

depends on the current, and also has a wide production spread and is temperature-dependant. So it is possible to have different V_P's during each half-cycle.

4-3-3 Number of primary turns, N_P

The number of primary turns, N_P, is fixed at transformer manufacture, and both halves of the primary and secondary should be very well matched. This becomes more difficult to achieve in medium and high power transformers [1]. Therefore, to a first order of approximation, this parameter can be assumed the same in each half-cycle. Whether or not the number of primary turns is equal, the primary wiring resistance may differ, which also contributes to flux imbalance.

4-3-4 Primary Leakage Inductance

So far, the effect of primary leakage inductance has been neglected. In practice, leakage inductance invariably exists, increases with the size of transformer, and is very much lay-out-dependant.

When one of the power switches is turned "on", a small voltage drop is produced across this inductance, which reduces the voltage applied to the primary. If the leakage inductance of one half of the primary circuit is not the same as that of the other half, which is generally the case, then different voltages will be applied across the primary, increasing the possibility of volt-second integral inequality.

4-3-5 Secondary Circuit

When both power switches are "off", both diodes, D_1 and D_2 in Fig. 4-2 conduct under the forcing action of the filter inductor, L. It has been assumed so far that the current in each diode during the dead time, the voltage drop across each diode, and the leakage inductance of each half of the secondary circuit are the same. In fact, each of the above values might be different, leading to some change in the flux during this period which may enhance saturation.

4-4 METHODS FOR OVERCOMING FLUX IMBALANCE

Several techniques exist for solving the flux imbalance in transformers which include [2]:

4-4-1 Inserting a Gap in the Core

This has the effect of shifting the knee of the hysteresis loop to a higher magnetic field strength, H, thus reducing the core sensitivity to waveform imbalance, since greater volt-second integral or magnetising-current-excursion imbalance is required to give the same core-flux imbalance. However, adding an air gap in the core has its own drawbacks, e.g. increased EMI, increased magnetising current and increased transformer size since the number of turns or cross-sectional area must usually be increased.

4-4-2 Adding Primary Resistance

If the primary current starts to increase in one direction due to a higher volt-second integral, a higher voltage will be dropped across any series resistance in the primary circuit. This reduces the voltage across the primary winding, thus tending to correct by reducing the volt-second integral in this direction. This solution has the effect of reducing converter efficiency especially at high currents, though.

4-4-3 Matching Power Transistors

This is to ensure that both power switches are matched in aspects of their performance which may lead to flux imbalance, such as storage times, V_{ON}, etc.
This solution is quite expensive, since two parameters should be matched; storage time and "on" voltage, and at all operating conditions. Also, this needs a special test set-up which is not always available when replacing transistors.

4-4-4 Using MOSFET's

Since MOSFET's exhibit little turn-off delay and switch very rapidly, as they are majority-carrier devices, any flux imbalance due to storage times differences virtually disappears when using MOSFET's. Another advantage when using MOSFET's is that if the MOSFET current increases, due to volt-second integral inequality, higher power across the device is lost causing the device to run at higher temperature. Increasing temperature causes the "on" voltage to increase, thus reducing the available primary voltage and tending to reduce the imbalance to some extent. The MOSFET also behaves as a small resistor when conducting, and thus also provides some correction as described in Sec. 4-4-2.

4-4-5 Applying Current-Mode Control

The most effective method to overcome flux imbalance is to sense the primary current by sensing the voltage drop across a small series resistance, and to switch the corresponding power switch "off" when this current increases beyond a certain limit. Although this method is being used effectively in practical systems, it has its own drawbacks which are discussed in some detail in the next section.

4-5 CURRENT-MODE CONTROL DRAWBACKS

Current-mode control is a very well established technique which was and still being used effectively in dc/dc converter design. Its advantages and disadvantages are thoroughly discussed and covered in literature [2, 3]. Five types of current-mode control exist and are briefly covered in [4].

The main form of current-mode control used throughout industry is the fixed-frequency, variable "on" time type, in which a voltage proportional to the sum of the primary current (the reflected load current plus the magnetising current) and the

compensating current (if one exists), is compared with a reference voltage. Once the sensed current signal increases above a reference level, a command is generated to terminate the "on" pulse, thus limiting the total primary current and, hence, the load current. The main advantage of this technique is that it provides both protection against over-current due to overload and/or core saturation. This adequately prevents the saturation problem frequently encountered in transformers due to voltage-second integral inequality, especially in push-pull dc/dc converters.

The main drawbacks of this technique are also covered in [2] and listed below:

1. Since the output voltage is proportional to the average inductor current, not the peak current, which varies with the d.c. input voltage, sensing the peak current may cause some momentary oscillation if the input voltage changes.
2. If the duty cycle is higher than 50%, this method of control becomes unstable.

To solve these problems, slope compensation is used.

One other drawback seems to exist at no- or light-load, and does not seem to be covered in literature. The following illustrates how this problem occurs.

If the current due to core losses is assumed negligible, the current monitored in the conventional current-mode control topologies, is the primary current, i_P, which comprises two terms: the reflected load current, i'_L, and the magnetising current, i_M, components.

It is well known that when saturation commences, the magnetising current (and not the load current) increases rapidly, and it is this current which should be isolated and sensed to indicate saturation. However, since it is not an easy task to separate these two components, the total current is used instead. This has the advantage of monitoring the load current and preventing it from exceeding a certain limit.

If the load current is not constant and changes between no-load and full-load current limits, the primary current, which has the same changes scaled by the turns ratio, will also change between the no-load and full-load current limits. In this case, the sensing circuit must be designed to sense the maximum expected primary current which is the load current reflected to the primary, plus the magnetising current, plus some margin which suits the application.

If the circuit is now working at no- or light-load, all or most of the primary current will be the magnetising current. Under this condition, when flux imbalance occurs,

the magnetising current will increase in one direction until it reaches the value at which the circuit is designed to terminate the "on" pulse. The maximum allowable current depends on the turns ratio as well as the load current, and increases if a step-up transformer is used, as the primary current in this case is higher than the secondary current. Although the current-mode control circuit, eventually, detects the current increase and prevents heavy saturation, it does not fully prevent slight flux imbalance in the transformer core. So under light-loads, the transformer core may be operated with quite severe flux imbalance. Under these conditions the circuit has several drawbacks which are now examined.

4-5-1 Reduced Power Throughput

The power which may be delivered through a transformer at any frequency can be given by Eq. (4-4) [5].

$$P = f_{SW} V_e \int_{B_L}^{B_H} H dB \tag{4-4}$$

where V_e is the effective transformer-core volume, f_{SW} is the switching frequency at which the transformer-core flux is changing, B_L is the minimum operating core-flux density and B_H is the maximum operating core-flux density.

Eq. (4-4) shows that the power delivered to the output is directly proportional to the switching frequency, effective core volume and the flux density excursion.

The term $\int_{B_L}^{B_H} H dB$ is the area enclosed by the operating hysteresis loop. As the core-flux density excursion decreases, as a result of flux imbalance, this loop area also decreases, thus reducing the power which the transformer can deliver.

4-5-2 Increased Transformer Core Losses

Transformer losses comprise core and copper losses. Core losses (hysteresis and Eddy-current) increase with increasing flux density as they are approximately proportional to the square of the flux density [6]. Hysteresis loss is proportional to the hysteresis loop area, which increases with flux density as follows [7]:

$$P_h = V_e \oint HdB \tag{4-5}$$

Eddy-Current loss, which is proportional to $(dB/dt)^2$ also increases with flux density as follows [7]:

$$P_e = \frac{d^2}{\rho} V_e (dB/dt)^2 \tag{4-6}$$

Copper loss, on the other hand, decreases with increasing flux density, since the number of primary turns and, hence, wire resistance is smaller for lower flux density in a given transformer design.

Fig. 4-4 shows that at some value of flux density there is minimum transformer losses.

If a transformer is designed for optimum flux density, and flux imbalance occurs, even if saturation does not occur due to current-mode control, then in one half cycle the flux density is higher than the optimum, and in the second half the flux density is lower than the optimum. When the flux density is higher, core losses increase. Also, because flux imbalance increases magnetising current, the copper loss will be higher, making average transformer losses higher and reducing the overall efficiency.

4-5-3 Different Currents in Each Power Switch

The primary current is unnecessarily allowed to have higher values in one direction and lower values in the other direction. This in turns, causes higher power loss in

one of the power switches and causes subsequent changes, in the long run, in the specifications of this switch compared to the other one.

4-5-4 Transient Effects

Since the transformer is operating at the beginning of the saturation region in one quadrant, it is very vulnerable to transients that can easily cause saturation.
These drawbacks are the price paid for sensing the primary and not the magnetising current. Therefore, to detect flux imbalance as it commences, irrespective of load current changes, the magnetising current should be sensed as described in the next section.

4-6 MAGNETISING-CURRENT-MODE CONTROL

The magnetising current can be obtained by subtracting the load current reflected to the primary, from the primary current. One way of achieving this is as shown in Fig. 4-5 by using a simple differential amplifier employing one operational amplifier.
The amplifier has two inputs; the first is the voltage drop across the sensing resistor R_{S1}, v_1, which is proportional to i_P (see Fig. 4-6); the second is the voltage drop across R_{S2}, v_2, which is proportional to i_L. By proper scaling of the two voltages, the output of the differential amplifier, v_M, will be proportional to i_M.
Fig. 4-6 shows a push-pull converter simulated in PSPICE and how magnetising current can be detected. The values of R_{S1} and R_{S2} should be as small as possible to reduce the power loss, but large enough to produce a signal which is significantly above the internal noise generated by the subsequent circuit. A few hundred millivolts above the noise or ripple level would be enough for this purpose. The op-amp should feature low offset voltage, low drift, and low noise, as the input voltages are relatively small.

If i'_S is the secondary current reflected to the primary, then from Fig. 4-6 the following can be written, assuming rectifier snubber currents have a negligible effect:

$$i'_S = N.\frac{v_2}{R_{S2}} \tag{4-7}$$

$$i_P = \frac{v_1}{R_{S1}} \tag{4-8}$$

$$i_M = i_P - i'_S = \frac{v_1}{R_{S1}} - \frac{Nv_2}{R_{S2}} \tag{4-9}$$

where N is the transformer turns ratio, $N = N_S / N_P$. If R_{S1} and R_{S2} are appropriately selected, such that $R_{S2} = NR_{S1}$, then:

$$i_M = \frac{1}{R_{S1}}(v_1 - v_2) \tag{4-10}$$

Since $R_1 / R_2 = R_3 / R_4$ in Fig. 4-6, then:

$$v_M = \frac{R_2}{R_1}(v_1 - v_2) \tag{4-11}$$

v_M may be expressed in terms of i_M as shown in Eq. 4-12.

$$v_M = \frac{R_2}{R_1} R_{S1} i_M = k i_M \tag{4-12}$$

where $k = \frac{R_2}{R_1} R_{S1}$.

Since v_M is proportional to i_M, if a preset v_M level is used to limit transistor "on" pulse widths, pulses may be terminated exactly at a specified magnetising current irrespective of load current changes to force uniform transformer core fluxing.

A closer examination of the currents in a push-pull converter, shows that during the "on" period of either switch, the secondary current reflected to the primary is simply

$i'_S = N \cdot i_S$, but during the "off" period of both switches, i.e. during the dead time, although there is no primary current, a secondary current is circulated by the energy stored in the filter inductor, which diodes D_1 and D_2 share (i.e. D_1 and D_2 conduct approximately $i_S / 2$).

Hence, during the dead time $i'_S \neq N \cdot i_S$, and the difference between the primary and the secondary current reflected to the primary, does not give the magnetising current. Furthermore, this difference equals to $-i'_S$, i.e. it is negative. Fortunately, during the dead time it is not necessary to sense the primary magnetising current since it is zero. Therefore, during this period the negative output of the differential amplifier can simply be ignored. It will be seen later (see Sec. 4-7-2) how this can be achieved practically.

This solution to the flux imbalance problem, is particularly useful in high power level systems when a step-up transformer is employed since relatively high values of primary current will be switched. This technique does not interfere with conventional voltage or current-mode control of power converters.

The circuit in Fig. 4-6 was simulated with two values of load resistance R_L, 2Ω and 1MΩ. The load current for the first case was 7 A, and for the second was about zero (no load). Fig. 4-7 shows the simulation results where v_M is exactly $10(v_1-v_2)$ as the gain of the op-amp is set to 10, and $v_M = 0$ during the dead time.

The next section describes an experimental push-pull converter that was designed and set up to demonstrate this method of equalising transformer-core flux excursions.

4-7 PUSH-PULL DC/DC CONVERTER DESIGN PROCEDURE

4-7-1 Transformer Design

4-7-1-1 Transformer specifications

The push-pull dc/dc converter was designed in the usual way [3] to meet the following specifications:

Input voltage 30 V, output voltage 5 V, output current 12 A, operating frequency 25 kHz. Transformer core size EC41/19/12, ferrite material grade 3C8, effective cross-sectional area is A_e = 121 mm^2. The maximum throughput power of the core is 150 W when used in a push-pull circuit switching at 25 kHz.

The range of transformer thermal resistance for the assumed core is (15.5 - 17) °C/W [3]. A value of 16 °C/W will be assumed.

4-7-1-2 Transformer power loss

If the thermal resistance, R_θ, is 16 °C/W, and the maximum permitted temperature rise, T_R, is 40 °C, the total internal dissipation, P_{ID}, is :

$$P_{ID} = \frac{T_R}{R_\theta} = \frac{40}{16} = 2.5 \quad \text{W}$$

For optimum efficiency and if copper loss, P_C, is 44% of total losses [3], the core loss should be $2.5 \times 0.44 = 1.1$ W.

4-7-1-3 Optimum flux density

From the data sheets at 1.1 W core loss and 25 kHz, the peak flux change $\Delta\phi$ is about 20 μWb. The area of the core is 121 mm^2. Therefore,

$$\Delta B = \frac{\Delta\phi}{A_e} = \frac{20 \cdot 10^{-6}}{121 \cdot 10^{-6}} \approx 165 \text{ mT}$$

4-7-1-4 Calculating secondary turns

The number of turns required for each volt is :

$$N/V = \frac{T_{ON}}{\Delta B \times A_e} = \frac{20}{0.165 \times 121} = 1.002 \text{ turns / Volt}$$

where the period of the switching cycle is 1/25 kHz = 40 μs , and the maximum possible T_{ON} (if the dead time is zero) for each half cycle is half of this period, or 20 μs.

If the efficiency of the converter is η=75 %, then the input power, P_{IN}, is :

$$P_{IN} = \frac{P_{OUT}}{\eta} = \frac{60}{0.75} = 80 \text{ W}$$

and the power loss will be 80-60=20 W.

If 80 % of this loss is in the secondary, then at 12 A (the maximum output current), the effective voltage drop on the secondary circuit is $(0.8 \times 20) / 12 = 1.33$ V.

The assumed maximum T_{ON} is 46 % of switching period for each transistor. The other 4 % is left as a dead time. For two transistors, the maximum on time is 92 % . Assuming negligible voltage drop across winding resistance, the minimum required transformer secondary voltage is :

$$V_S = (5 + 1.33) / 0.92 = 6.88 \text{ V}$$

The secondary turns now can be calculated :

$$N_S = 6.88 / 1.002 = 6.866 \text{ turn}$$

The assumed secondary turns is $N_S = 7$.

4-7-1-5 Calculating primary turns

Primary turns should be calculated depending on the maximum input voltage. In this design $V_{IN(\min)} = 25$ V is assumed.

The calculated turns per volt is now $6.88 / 7 \approx 0.98$ rather than 1.002 which was first assumed. Therefore, primary turns is calculated as:

$$N_P = 25 / (6.88 / 7) \approx 25.4 \text{ turns}$$

The assumed primary turns is $N_P = 25$ turns.

4-7-1-6 Splitting primary turns

In order to investigate the flux imbalance problem, one of the following parameters should be changed : N_P, V_P or T_{ON}. In our case it is not possible to change T_{ON} separately for each transistor since it is defined by the control circuit. V_P, on the other hand, is fixed by the d.c. supply voltage and the voltage drop across the switch [see Eq. (4-3)] and can not be deliberately changed for each primary winding circuit unless, of course, a resistor or a diode is connected in series with one half of primary winding to reduce the voltage drop across that half. This, however, would cause high power loss if the primary current is high. The only practical parameter which can be used for flux imbalance investigation is N_P. Therefore, one half of the primary, N_{P1}, is wound with 25 turns, the other half , N_{P2}, was split into two windings of 20 turns and 5 turns. these two parts of N_{P2} are connected in series for normal operation. To create flux imbalance, the 5-turn winding is removed and the transformer then operates with $N_{P1} = 25$ and $N_{P2} = 20$.

4-7-2 Control Circuit Design

Fig. 4-8 shows the schematic diagram of the complete push-pull dc/dc converter. A voltage-mode control circuit (U_1 = SG3525A) is used to demonstrate how the flux imbalance problem occurs at light-load. The shut-down input, SD (Pin 10), is used to terminate the "on" pulse when the primary *or* the magnetising current reaches a

certain limit. The *or* function is achieved by D_3 and D_4. All other components around the control circuit are designed as recommended by Unitrode [5].

Three feedback loops exist: the first is used to maintain the output voltage constant through the voltage divider R_1 and R_2; the second is used to sense the primary current by sensing the voltage drop across R_3 and terminate the output signal when the current exceeds a threshold voltage set by R_4 and R_5; and the third is to sense the load current and subtract it from the primary current (after scaling), such that the resulting signal is proportional to the magnetising current. When the magnetising current reaches a limit defined by R_6 and R_7, the control circuit is shutdown thus preventing any further increase in the magnetising current. A low noise operational amplifier, OPA27GP, is used to generate a signal proportional to the magnetising current, and is designed as recommended by Burr-Brown [8].

During the conduction periods of Q_1 and Q_2, the primary current is higher than the reflected secondary current. In this case, the output of U_3 is proportional to the magnetising current. During the dead time, this value is negative as described earlier, and the output of U_2-B in this case will be negative and has no effect on the shutdown pin of the control circuit and it is simply ignored.

Switches S_1 and S_2 are used to apply the two control methods (sensing the primary current and sensing the magnetising current) separately or together. Resistor R_8 should be connected between the shutdown pin and ground should S_1 and S_2 are left open, since pin 10 should not be left unconnected [5]. All power supply inputs to the IC's were decoupled by 100 nF ceramic capacitors very close to the power supply pins.

4-7-3 Current Transducer Connections

The current transducer used to sense the load current is an existing Hall-Effect transducer type LTA 50 P/SP1, with a ratio of 1:1000 from LEM [9]. It is designed to measure a maximum current of 50 A. When used as a current transducer, its connections are as shown in Fig. 4-9. Decoupling capacitors should be connected between pins 2 and 6, and between these two pins and ground. The internal 100 Ω

resistor can be used to produce a voltage proportional to the output current, but in the designed circuit another external resistor was used which is calculated as follows : From Fig. 4-8, the following can be written :

$$v_1 = R_3 i_P = R_3 (i'_S + i_M) = R_3 i'_S + R_3 i_M \tag{4-13}$$

where $i'_S = N i_S$ is the reflected secondary current and $N = \frac{N_S}{N_P}$.

$$v_2 = \frac{R_9 i_S}{1000} = \frac{R_9 i'_S / N}{1000} \tag{4-14}$$

If Eq. (4-14) is subtracted from Eq. (4-13) after selecting R_9 such that

$$R_9 = 1000 N R_3 \tag{4-15}$$

a formula for i_M can be obtained:

$$i_M = \frac{v_1 - v_2}{R_3} \tag{4-16}$$

R_3 is chosen 0.235 Ω, which gives $R_9 = 65.8\,\Omega$.
The difference v_1-v_2 is multiplied by the gain of the operational amplifier, 100k / 1.8k, to get a reasonable output voltage signal.

4-7-4 Avoiding Series Sensing Resistors

It is possible to avoid having to use sensing resistors such as R_3 in Fig. 4-8 by using a Hall-effect current transducer if the turns ratio, N, is carefully selected. If, say, N = 1/4, then four turns of a wire conducting the primary current are passed through the transducer in one direction, and one turn of a wire conducting the secondary current is passed in the other direction as shown in Fig. 4-10.

The resulting induced magnetic field, and hence the output of the current transducer, is proportional to the magnetising current only. Quantitatively, the output current will be $4i_M$ since 4 turns of the wire holding the primary current are wound on the transducer. During the dead time, the output of the current transducer is negative and, as described earlier, has no effect on the control circuit.

In this case, the current transducer is expected to give a small output current since i_M is small. Therefore, if series sensing resistors are to be avoided, the chosen current transducer should be able to measure small currents with the required accuracy. The existing current transducer did not meet these requirements, therefore this approach was not followed. Alternatively, the number of windings on the transducer can be increased to increase the output signal.

4-7-5 Experimental Results

The circuit shown in Fig. 4-8 was tested practically. At the beginning S_1 and S_2 are left open and only an output voltage feedback is used to control the output voltage. The circuit exhibits flux imbalance when switch S_2 is open, as shown in Fig. 4-11. This was seen at 12 A load current. When S_2 is closed, i.e. the primary current is sensed, the flux imbalance disappeared, as shown in Fig. 4-12, and the same amplitude of magnetising current is shown in each half cycle. The load current has been reduced slowly until the voltage across R_3 (which is an indication of primary current) decreased below the threshold voltage set by R_5 (the inverting input of U_2-A). At this time the flux imbalance appears again, as shown in Fig. 4-13, and it is clearly seen the difference in magnetising current in alternate half cycles. Now there is no effect of S_2 whether it is open or closed.

The load current has been further decreased to about 3 A while the flux imbalance is still seen, at which time switch S_1 is closed. The magnetising current now is seen to have the same amplitude in alternate half cycles, as shown in Fig. 4-14. Reducing the current further has no effect on the shape of the magnetising current since it is subtracted from the primary current.

The same is applied using a current-mode control IC (UC3846) designed as recommended in [5] to work at about 40 kHz, as shown in Fig. 4-15. At heavy

loads, although deliberate flux imbalance is used, the peak primary current is the same each half cycle. At light loads, the flux imbalance appears and the transformer saturates in one direction. This has been seen as an upwards concavity on the ramp of the primary current waveform in each second half cycle.

It is worth noting here is that any improper scaling of the currents, the subtraction will not give a component proportional to the magnetising current. In this case there will be some effect of load current changes on the magnetising current, but if the error in scaling currents is small, the change in magnetising current can be ignored.

Fig. 4-16 shows photographs for the practical push-pull dc/dc converter together with the test setup.

4-8 FLUX IMBALANCE IN OTHER DC/DC CONVERTERS

Flux imbalance can also occur in other dc/dc converters that use the upper and lower half of the hysteresis loop, such as half- and full-bridge converters.

Half-bridge circuits employ two series capacitors to provide a point which holds half the d.c. supply voltage. If the values of these two capacitors are not identical, the junction between them will not be at half the supply voltage. This applies different voltages at the primary in each half cycle, thus increasing the possibility of flux imbalance. To solve this problem in half-bridge circuits, which are used at relatively low power, a small non-polarised capacitor can usually be placed in series with the primary to stop the d.c. bias caused by the flux imbalance.

In full-bridge converters, flux imbalance can still occur, but it is less likely than in half-bridge circuits [2] since the former do not have the two series capacitors, especially if MOSFET's are used.

One advantage of half- and full-bridge circuits over push-pull ones, is that the flux imbalance in the latter caused by the difference in primary winding turns and its resistance do not occur in the former, as the power transformer used has only one primary winding.

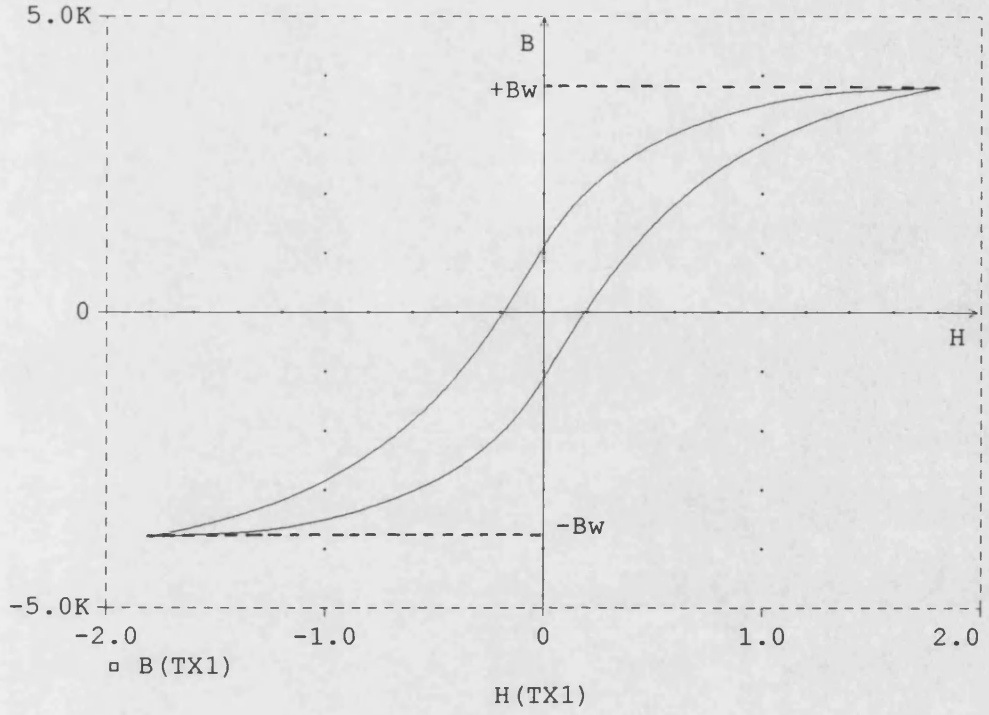
4-9 CONCLUSION

One of the main drawbacks of push-pull power-converter circuits is flux imbalance, which can be solved using current-mode control. Since the power device current is limited, it is safe but not very efficient since the main power device(s) are having to switch a high magnetising current. Therefore, magnetising-current-mode control may be used, in which the maximum switch duty-cycle is electronically limited so that a predetermined value of magnetising current is not exceeded irrespective of load current changes. This forces a uniform transformer core fluxing.

This technique can be combined with conventional current-mode control if primary current protection is required.

A push-pull converter use both primary and magnetising current mode control has been designed and practically tested. The results show that at light load, flux imbalance is still a possibility when detecting only the primary current. When the magnetising current is used, the flux imbalance is eliminated even at light- or no-load.

a)



b)

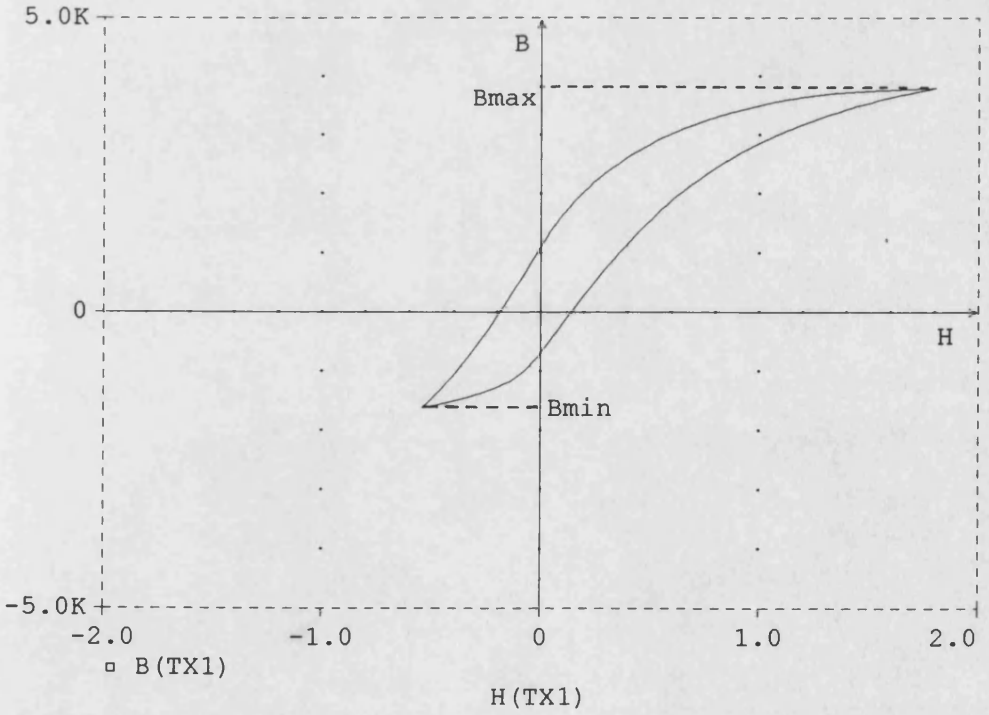


Fig. 4-1 Hysteresis loops for: a) symmetrical core operation and b) asymmetrical core operation

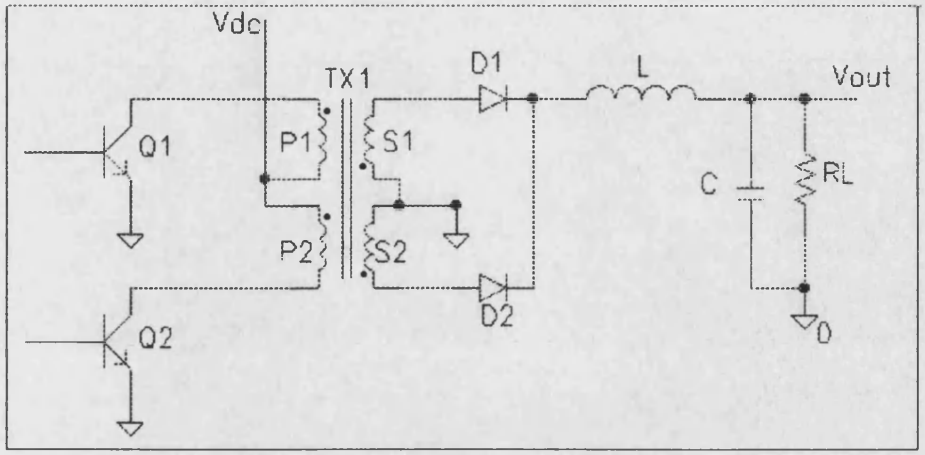
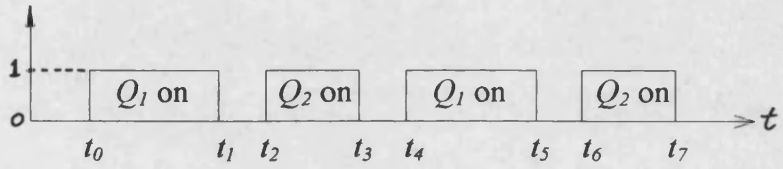


Fig. 4-2 The power stage of a push-pull converter

a)



b)

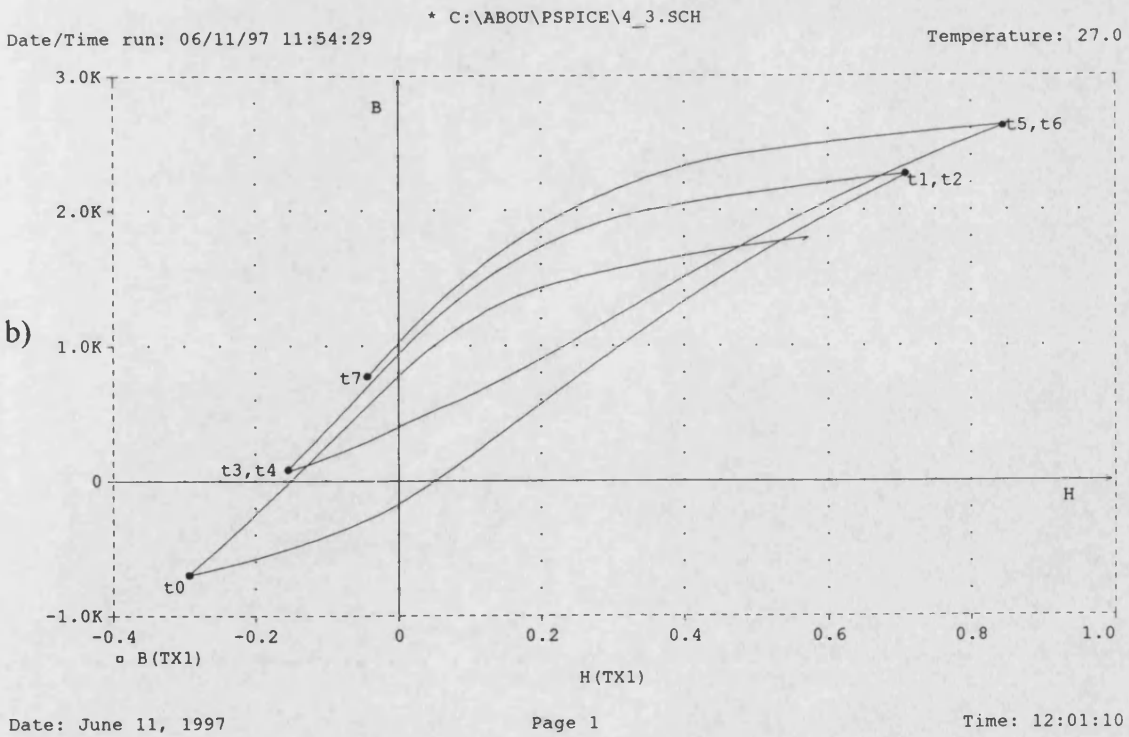


Fig. 4-3 a) Unequal turn-on pulses and b) the associated hysteresis loops which move slowly into saturation due to volt-second integral inequality

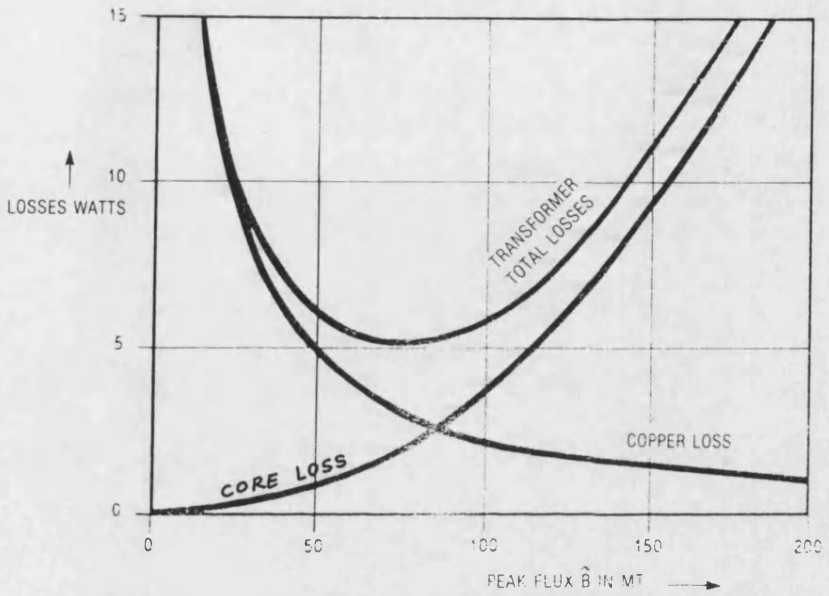


Fig. 4-4 Transformer losses versus flux density [3]

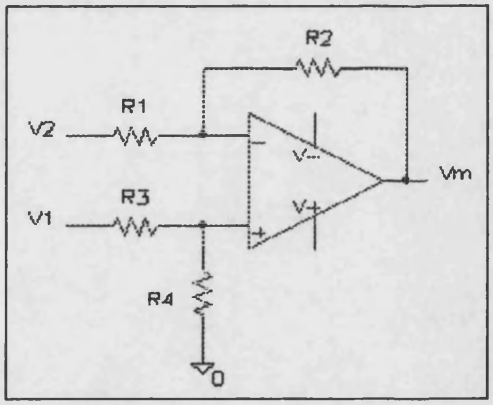


Fig. 4-5 A differential amplifier employing one op-amp

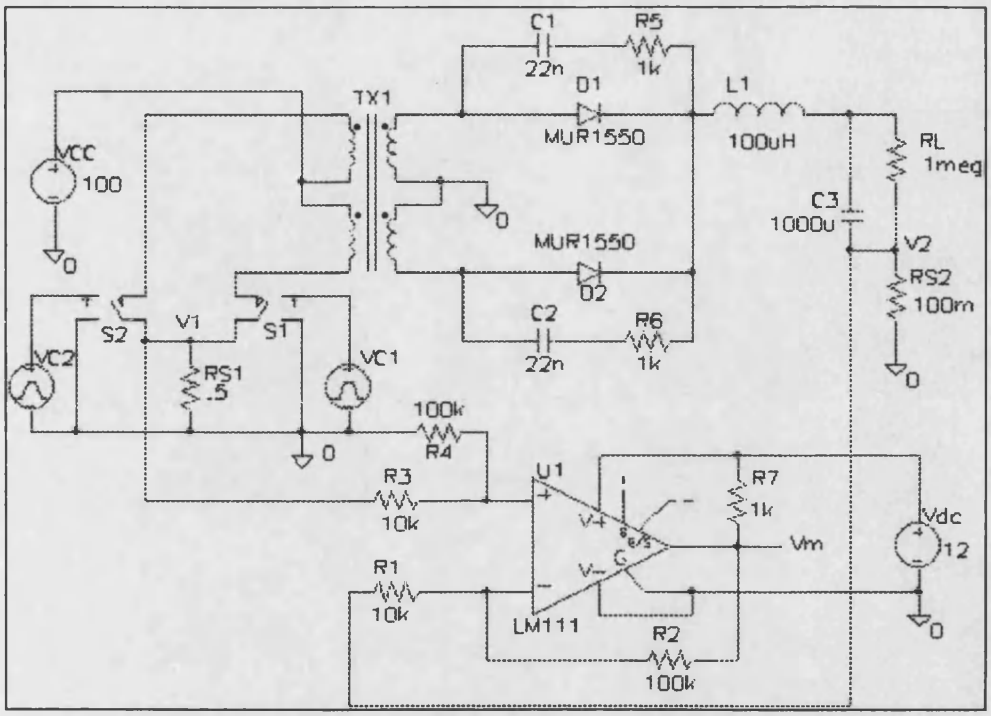


Fig. 4-6 Sensing magnetising current in push-pull converters

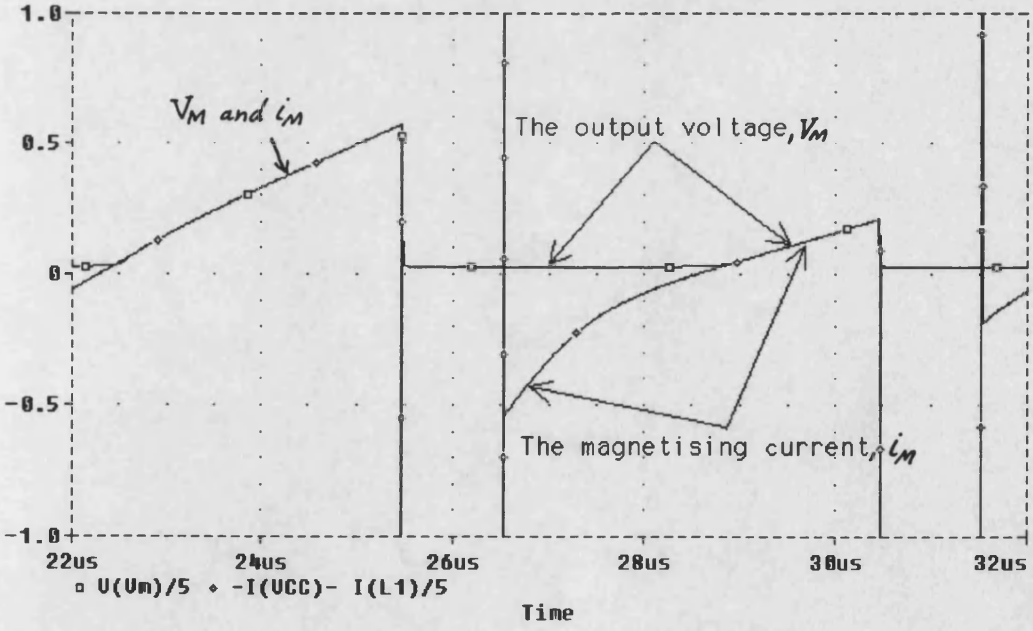


Fig. 4-7 The magnetising current and output voltage of the differential amplifier for the simulated circuit of Fig. 4-6

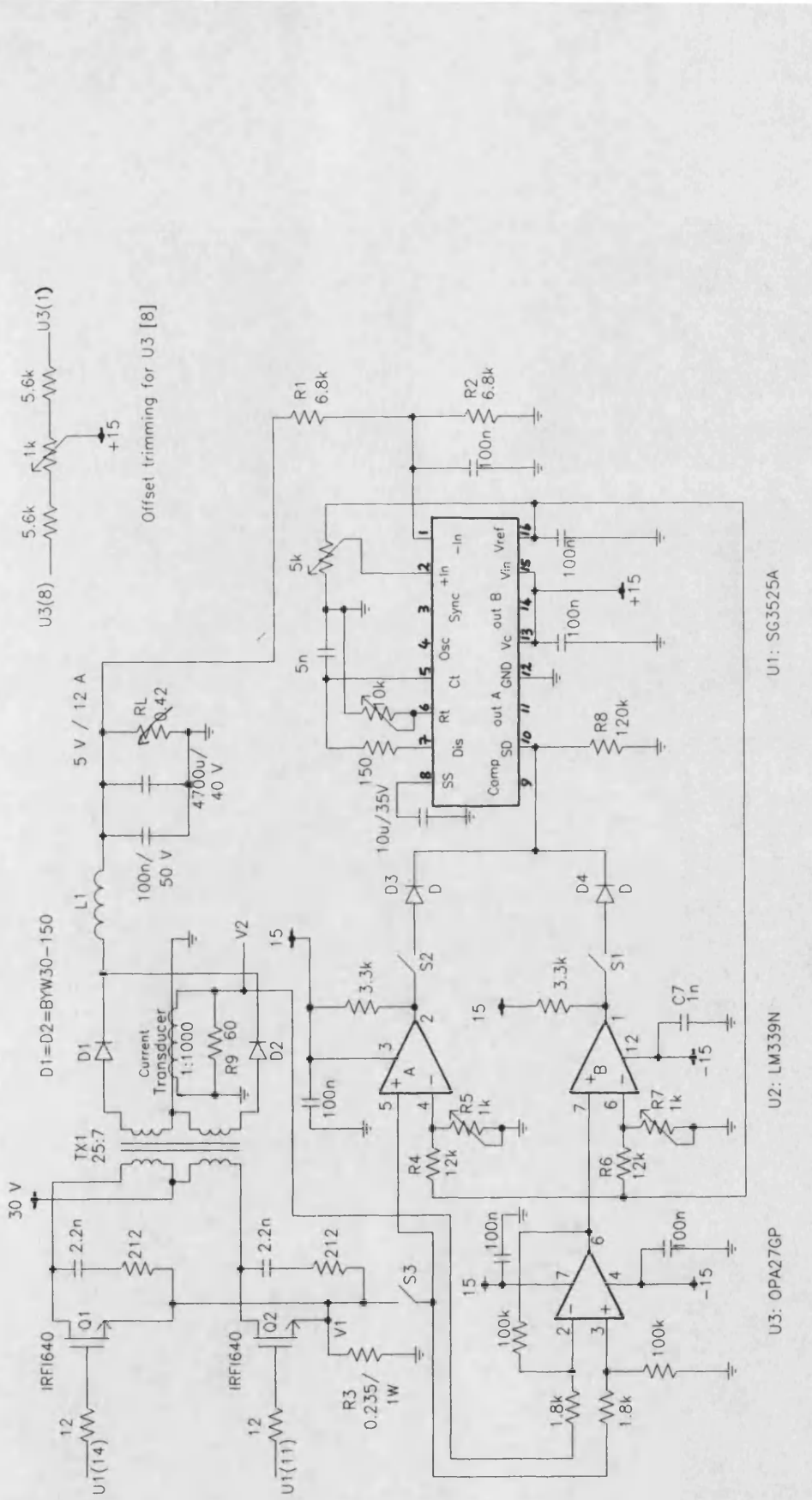
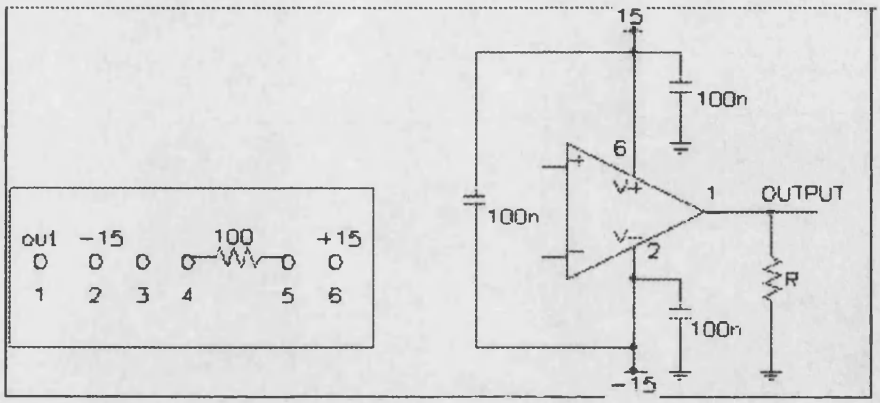


Fig. 4-8 A push-pull dc/dc converter used to investigate flux imbalance



a) Internal b) External

Fig. 4-9 Current transducer connections

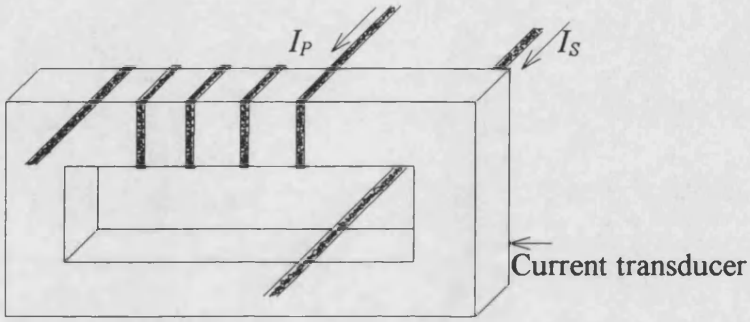


Fig. 4-10 Avoiding series resistance by using only a current transducer to subtract the load current from the primary current

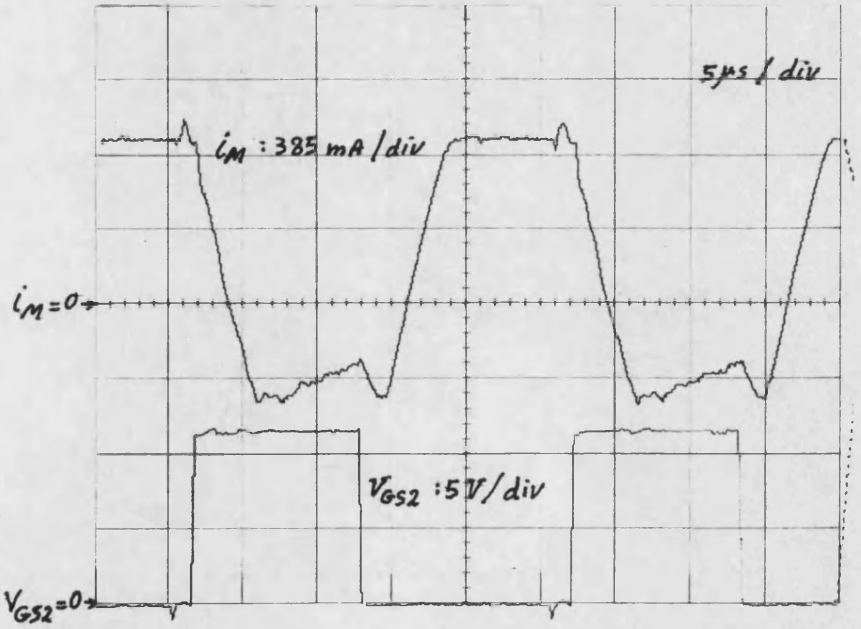


Fig. 4-11 Transformer magnetising current showing core flux imbalance: no current-mode control is used

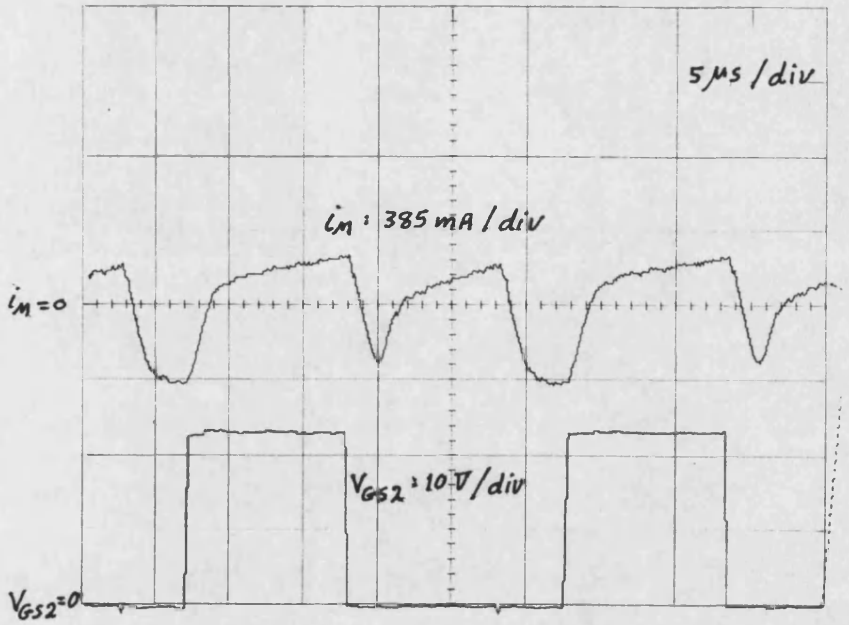


Fig. 4-12 Transformer magnetising current showing no core flux imbalance at 12 A load current when current-mode control is used

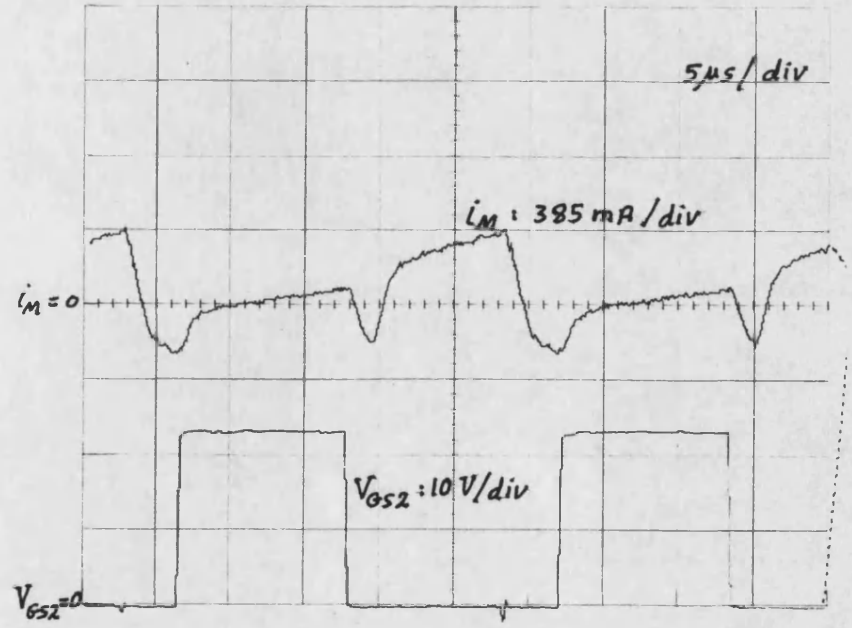


Fig. 4-13 Transformer magnetising current showing core flux imbalance at 3 A load current even when current-mode control is used

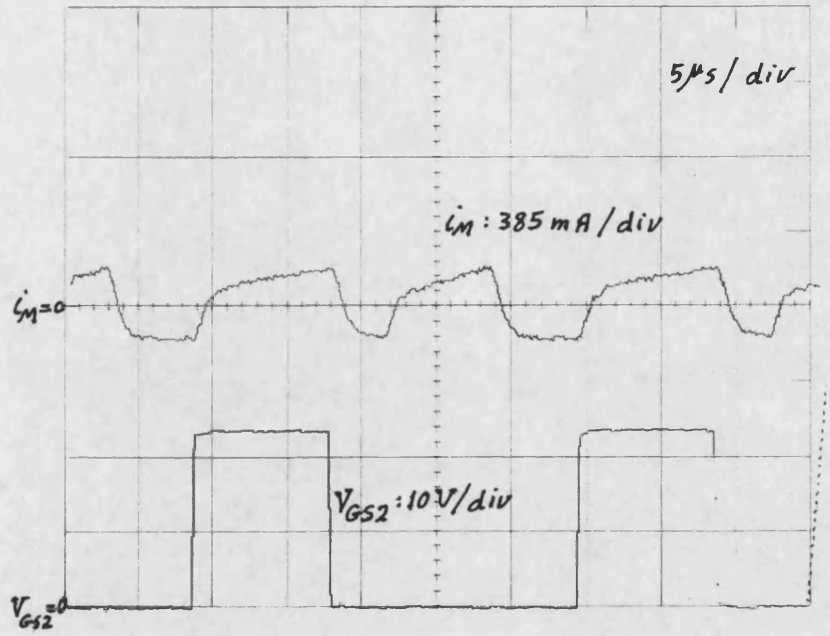


Fig. 4-14 Transformer magnetising current showing the absence of flux imbalance when magnetising-current-mode control is used even at light loads

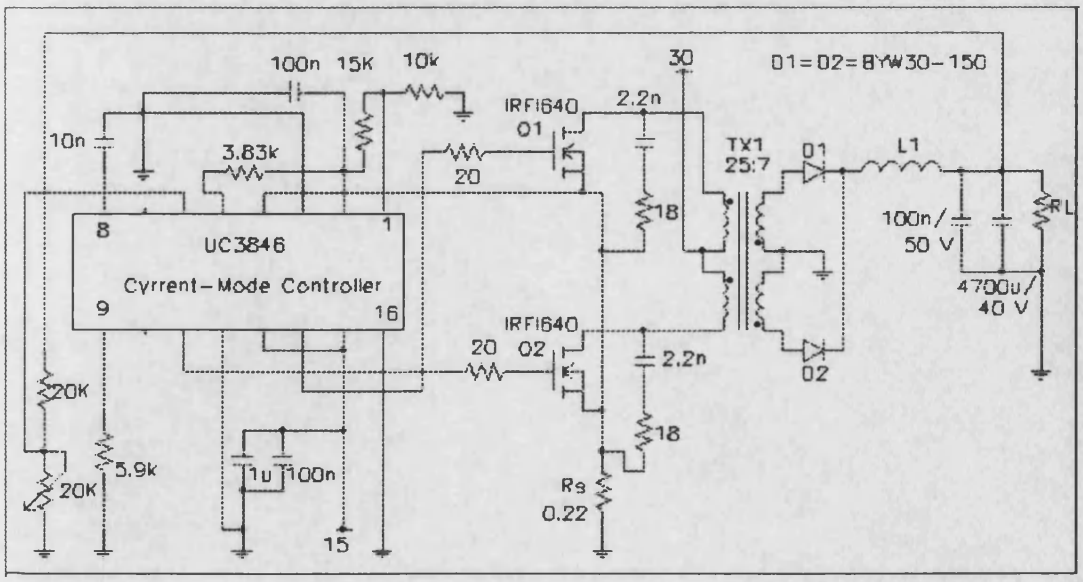
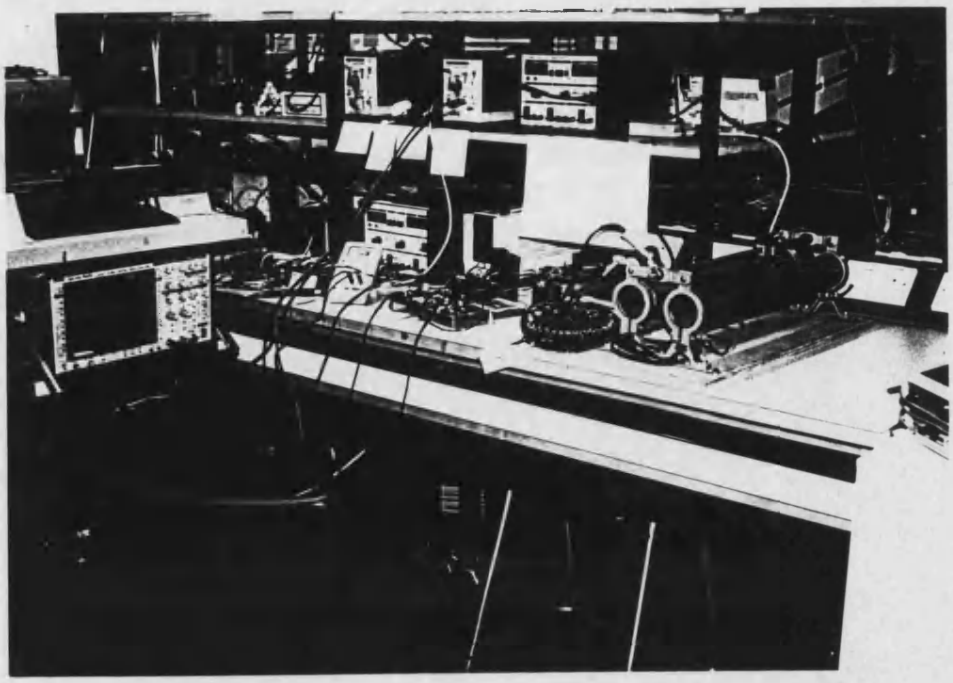


Fig. 4-15 Push-pull dc/dc converter using current-mode control

a)



b)

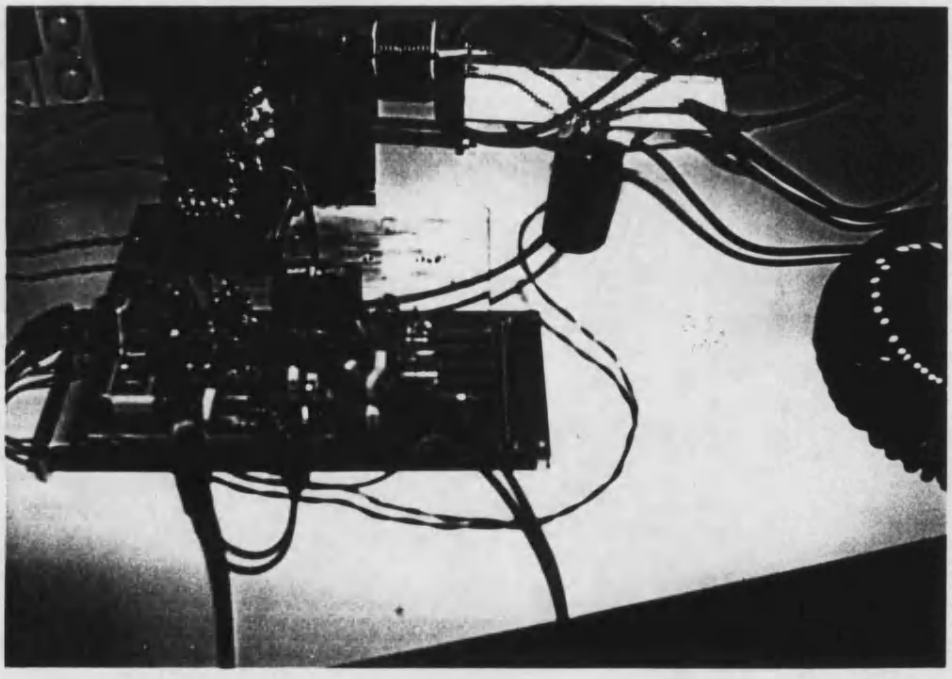


Fig. 4-16 Photographs for the practical push-pull dc/dc converter with the test setup

CHAPTER FOUR REFERENCES

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PUSH-PULL DC/DC CONVERTER USING THREE-PHASE TRANSFORMER

5-1 INTRODUCTION

Transformers are relatively heavy components, which occupy a lot of space and are costly. Therefore, it is desirable to reduce their size or even to eliminate them from circuits wherever possible. Unfortunately, in many power electronics systems, transformers are likely to remain essential, and hence future converter power density improvements necessitate further reduction in transformer size and weight through better optimized transformer design, improvement in core material, or novel converter topologies.

Three-phase transformers, as will be seen in details in Ch. 14, have less weight and size compared with three single-phase transformers that deliver the same power.

Therefore, the application of using three-phase transformer in dc/dc converters has been examined in the hope of achieving an overall improvement in power density. The idea is found to be easily applied on push-pull converters.

Fig. 5-1 shows a three-phase transformer, with primary and secondary voltages and the flux phasing in each limb.

The idea of employing a three-phase transformer in dc/dc converters, is to apply three voltage pulses across the three primary windings alternately in such a way that the flux in each limb changes from point 3 to point 1 on the hysteresis loop (see Fig. 5-2) when the pulses are applied to the associated primary windings in turn. During a

second pulse, the flux in the appropriate limbs moves down from point 1 to point 2, and during a third pulse, the flux moves further down from point 2 back to point 3. These cyclic changes in limb-fluxes ϕ_2 and ϕ_3 lag ϕ_1 by 120° and 240°, respectively. If this can be realized, then each time one of the limbs is active, the flux in this limb changes from $-B_{max}$ to $+B_{max}$, making an excursion of $2B_{max}$. In this case, the limb is fully utilized and a maximum power throughput is obtained since the power which the transformer can deliver is given by:

$$P = V_e \cdot f_{SW} \int_{-B\max}^{B\max} HdB \qquad (5\text{-}1)$$

where P is the available power for transfer [W],

V_e is the effective core volume [m^3],

f_{SW} is the switching frequency [Hz],

$-B_{max}$ and B_{max} are the minimum and maximum flux densities [T], and

H is the magnetic field strength [A/m].

For more details on effective and actual core parameters, see App. (5).

5-2 PRINCIPLE OF OPERATION

The circuit shown in Fig. 5-3 is used to describe the principle of operation of using a three-phase transformer in dc/dc converters.

Let us assume that the flux in the first limb is $-B_{max}$, in the second limb is zero, and in the third limb is $+B_{max}$ (points 3, 2 and 1 in Fig. 5-2, respectively). Let us also assume that switch Q_1 is turned "on" at time t_0 = 0 as shown in Fig. 5-4a. The primary voltage v_{P1} will be effectively V_{DC} ignoring the voltage drop across Q_1. This constant voltage produces a flux ϕ_1 in the first limb given by:

$$\phi_1 = -\frac{1}{N_P}\int_{t_0}^{t_1} v_{P1}dt = -\frac{V_{DC}}{N_P}(t_1 - t_0) \qquad (5\text{-}2)$$

The maximum $T_{ON} = t_1\text{-}t_0$ and the primary turns are chosen to achieve the maximum required $B_{max} = \phi_{max} / A_e$. In this case, the change in the flux in the first limb is from $-\phi_{max}$ to $+\phi_{max}$ or $2\phi_{max}$. This flux flows upwards in the first limb, and returns in limbs 2 and 3. Assuming symmetrical magnetic paths, the flux will be divided equally between limbs 2 and 3, making a change of ϕ_{max} in each limb. The flux in the second limb moves from zero to $-\phi_{max}$, while that in the third limb moves from $+\phi_{max}$ to zero.

Ignoring the voltage drop across the power switch, the voltage across the first primary, v_{P1}, is approximately V_{DC}. Because the flux in the second and third limbs is half of the flux in the first limb and in the opposite direction, the voltage induced at the second and third primary windings due to this flux is half of that across the first primary winding and in the opposite direction, i.e. $-V_{DC}/2$. Therefore, the voltage across power switches Q_2 and Q_3 is:

$$v_{DS2} = v_{DS3} = V_{DC} - (-\frac{V_{DC}}{2}) = 1.5V_{DC} \qquad (5\text{-}3)$$

The secondary voltages will be the same as the primary voltages but scaled by the turns ratio such that D_1 conducts while D_2 and D_3 are reverse-biased and cut off.

During the second pulse, primary P_2 is active. The flux in limb 2 changes from $-\phi_{max}$ to $+\phi_{max}$, the flux in limb 3 changes from zero to $-\phi_{max}$ and the flux in limb 1 changes from $+\phi_{max}$ to zero. During this second pulse, D_2 conducts while D_1 and D_3 are cut off. The voltage across the first and third primary windings will be $-V_{DC}/2$ and that across Q_1 and Q_3 is 1.5 V_{DC}.

The same is also applied for the third limb during the third pulse.

Fig. 5-4b shows the expected flux in each limb, Fig. 5-4c shows one of the primary voltages, and Fig. 5-4d shows the expected voltage across the power switches.

5-3 THE CONTROL CIRCUIT

Fig. 5-5 shows the circuit used to generate the three driving signals for the three-phase push-pull dc/dc converter. The principle of operation is as follows:

U_1 generates the switching frequency which produces the sawtooth signal, V_{ST}, as shown in Fig. 5-6a. R_4, R_5 and C_2 (see U6-A) are chosen to produce an approximately linear sawtooth signal, V_{ST}, which is compared with a reference voltage, V_{REF}, defined by R_8 and R_{V2} which sets the pulse width at pin 2 of U6-A, as shown in Fig. 5-6b. R_{V1} is used to control the switching frequency, and C_5 is used to generate a soft start.

U2-A and B generate two clock signals, CLK_1 and CLK_2, as shown in Fig. 5-6c and d with the falling edge of CLK_1 generating CLK_2. CLK_1 and CLK_2 are applied to a set of D-type flip-flops to generate the 3-phase 120° displaced driving signals as follows:

On start-up, the non-inverting input of U5-B is lower than the inverting input, causing the output to be low. This causes the output of U3-B and U4-A to be high, while all other outputs of the D-type flip-flops are low. Also, the output of U7-D will be low, forcing all outputs V_1, V_2 and V_3 to be low, which is the start-up state of the control circuit. CLK_1 and CLK_2 at this time have no effect on the outputs of the flip-flops. C_3 charges through R_{11}, and when the voltage across it increases slightly above 6V, the output of U5-B takes the supply voltage (12V). This causes the output of U7-D to follow V_{SW}. If at this moment V_{SW} is high, V_1 switches high and V_2 and V_3 remain low. If it is assumed that it is the turn of CLK_1 pulse, "zero" will be transferred from the input of U3-B to its output, and "one" will be transferred from the input of U4-B to its output. If now V_{SW} is high, V_2 will be high, while V_1 and V_3 will be low. This stays until the second pulse of CLK_1. When CLK_2 switches high, "one" will be transferred to the output of U5-A and "zero" to the output of U4-A, while the output of U3-A stays "zero". If now V_{SW} is high, V_3 will be high and V_1 and V_2 will be low, and the waveforms shown in Fig. 5-6e, f and g are obtained. The same argument is applied if it is assumed that CLK_2 comes before CLK_1.

From the above, it can be seen that two outputs cannot be high at the same time.

Table 5-1 lists the integrated circuits used in the control board.

Symbol	Type-number	Function
U1	CA555CE	Timer
U2	MM54C221N	Dual monostable multivibrator
U3-5	MM74C74N	Dual D-type flip-flop
U6	LM139J	Quad comparator
U7	MM74C08N	Quad 2-input AND gate
U8	MM74C04N	Hex inverters
U9,10	ICL7667CPA	MOSFET driver

Table 5-1 The integrated circuits used in the control board

5-4 PRACTICAL WAVEFORMS

5-4-1 A Pure Resistive Load

To test the idea of using a three phase transformer in dc/dc converters, the circuit shown in Fig. 5-7 was used. In order to test the basic operation of the circuit, a purely resistive load was first assumed to be connected. Fig. 5-8 shows the driving signals V_1, V_2 and V_3 which are generated from the control circuit shown in Fig. 5-5.

5-4-1-1 The specifications of the circuit

Switching frequency, f_{SW}= 20 kHz, with a switching period, T_{SW} = 50 μs,

Input voltage, V_{DC} = 100 V,

Pulse width, P_W = 11.2 μs,

Load resistance, R_L = 18 Ω on each output.

$Q_1 = Q_2 = Q_3 =$ MOSFET type IRFP450 (500V/13A),

Three-phase transformer: core size EC70, material grade: 3C80, N_P = 45 turns, N_S = 11 turns, and 3-star connected winding pairs.

5-4-1-2 Practical waveforms

Fig. 5-9 shows the driving signal, V_1, the drain-source voltage, V_{DS1}, and the secondary voltage, V_{S1}. The amplitude of the control signal V_1 is 12V with a pulse width of 11.2 μs.

When V_1 is high, Q_1 is "on", and V_{DS1} is almost zero. The total supply voltage V_{DC} is applied to the primary P_2, and is transformed by the turns ratio to the secondary. The output V_{S1} will be:

$$V_{S1} = V_{DC}\frac{N_S}{N_P} = 100 \times \frac{11}{45} = 24.4 \text{ V} \qquad (5\text{-}4)$$

When the control signal V_1 falls to zero, Q_1 is turned "off" and the voltage across it, V_{DS1}, increases to V_{DC} = 100 V (time period t_1 to t_2). At $t = t_2$, Q_2 is turned on and, as described earlier, V_{DS1} increases to:

$$V_{DS1} = 1.5\ V_{DC} = 1.5 \times 100 = 150 \text{ V} \qquad (5\text{-}5)$$

When Q_2 transfers to "off" at $t = t_3$, V_{DS1} becomes V_{DC} = 100 V. At $t = t_4$, Q_3 is turned "on" and V_{DS1} also takes 150V until $t = t_5$, at which time Q_3 becomes "off" and V_{DS1} = 100V . At $t = t_6$ the whole cycle repeats.

Ignoring the overshoot in V_{DS1}, and the very small shift of the waveform downwards (which may be due measurement errors), it may be seen that there is some similarity with waveform, V_{DS1}, shown in Fig. 5-4d. The overshoot of V_{DS1} waveform shown as rounded edges may be due to resonance between the transformer primary leakage inductance and the capacitance of the power switches and snubber capacitance of the output rectifier diodes.

Concerning V_{S1} in Fig. 5-9, when Q_1 is "on", $V_{S1} \approx$ 24V, as calculated in Eq. (5-4). When Q_1 is "off" (time period t_1 to t_2), V_{S1} = 0. When Q_2 or Q_3 is "off", V_{S1} becomes

half of its value when Q_1 is "on", i.e. $V_{S1} \approx 12V$. Also, V_{S1} in Fig. 5-9 resembles the ideal V_{S1} in Fig. 5-4c.

Fig. 5-10 shows the three outputs together with one of the driving signals, V_1, while Fig. 5-11 shows the input current I_{IN} absorbed from the input voltage V_{DC}.

5-4-2 Rectified and Filtered Output

Fig. 5-3 shows the practical push-pull converter using a three-phase transformer. The specifications for the circuit are largely described above. In addition:

$D_1 = D_2 = D_3$ = BYW30-150 (12A/150V) fast recovery rectifier,

L = 1.5 mH, C = 4600 μF with R_{ESR} = 40 mΩ, R_L = 9.2 Ω.

Fig. 5-12 shows different waveforms for the circuit shown in Fig. 5-3

Further examination of the circuit shown in Fig. 5-3 shows that during the "on" time of, say, Q_1, the flux in the first limb increases linearly at a rate defined by V_{DC} / N_P. In this case, D_1 conducts since V_{S1} is positive, and passes a current to the load, while L stores energy given by $1/2LI^2T_{ON}$ (assuming constant load current, I).

During the same "on" time of Q_1, the change in the flux in the other two limbs will be, in theory, half of the flux in the first limb and in the opposite direction. Therefore, the voltages V_{S2} and V_{S3} induced in the other two secondaries will be half V_{S1} and in the opposite direction. D_2 and D_3 are therefore reverse-biased.

At the end of this "on" period, Q_1 opens. In this case, the energy stored in L forces the current to keep flowing in the same direction. This causes all diodes $D_{1\text{-}3}$ to conduct and share the load current such that each diode and the associated secondary conduct almost $I/3$. The same explanation that applies to single-phase push-pull converter operation during this phase (see Sec. 2-1-1) also applies here. That is, the flux during the dead time is virtually constant. Therefore, no voltage is induced at the secondary windings and, hence, at the primary windings. Therefore, V_{DS} equals to V_{DC} during the dead time.

5-5 ADVANTAGES OF THREE-PHASE PUSH-PULL CONVERTERS

1. The main advantage of this circuit, as has been described, is that the power switches operate at drain or collector stress voltage of about $1.5V_{DC}$ compared to $2V_{DC}$ in single-phase push-pull converters. Therefore, this topology is favored for off-line applications over the conventional push-pull circuits.
2. Since three output pulses exist in one complete switching cycle, the output voltage ripple is less than that in conventional push-pull circuits where only two pulses exist. In other words, for the same output ripple level, the required filter size will be smaller.
3. Since three switches and three diodes are used, the average current per device is smaller. Therefore, when the limiting factor is the average current, this circuit can handle higher load currents.

5-6 DISADVANTAGES OF THREE-PHASE PUSH-PULL CONVERTERS

1. The main disadvantage of the proposed circuit is that one primary is active at a time. Hence, the primary winding utilization of the transformer is less than that in the conventional push-pull circuits.
2. The same also applies for the power-semiconductor switches and rectifiers.
3. For a given output power, switching losses are slightly higher($\approx 13\%$) than the normal push-pull converters because three switches and diodes are active in each cycle. However, the conduction power loss is virtually the same.
4. This converter is likely to be more expensive than normal push-pull converters given its greater complexity and non-standard transformer geometry.

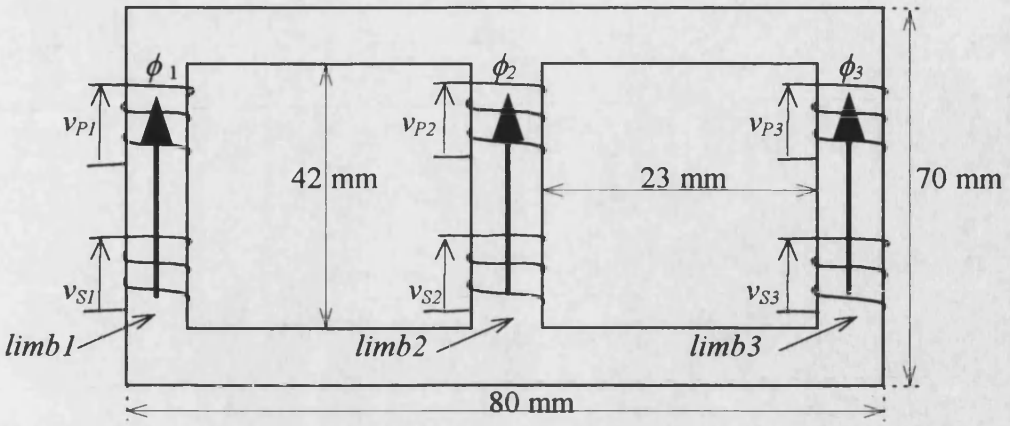

Fig. 5-1 A three-phase transformer showing voltage and flux positive directions

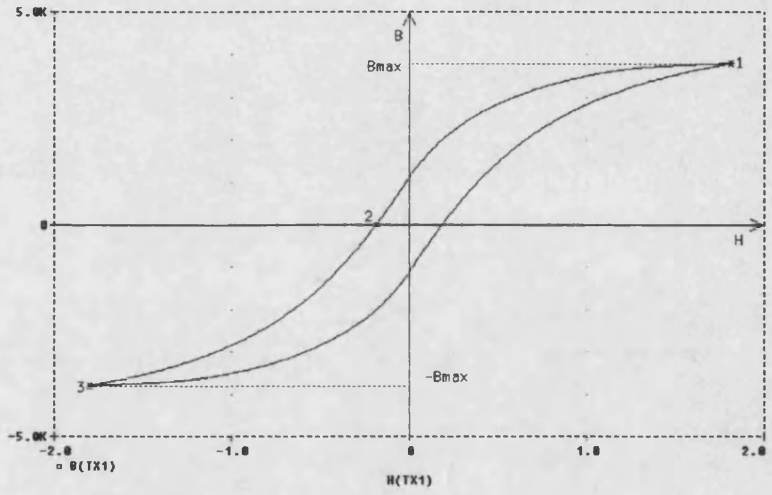

Fig. 5-2 Hysteresis loop showing the expected positions of flux densities in each limb in a three-phase converter working in a push-pull circuit

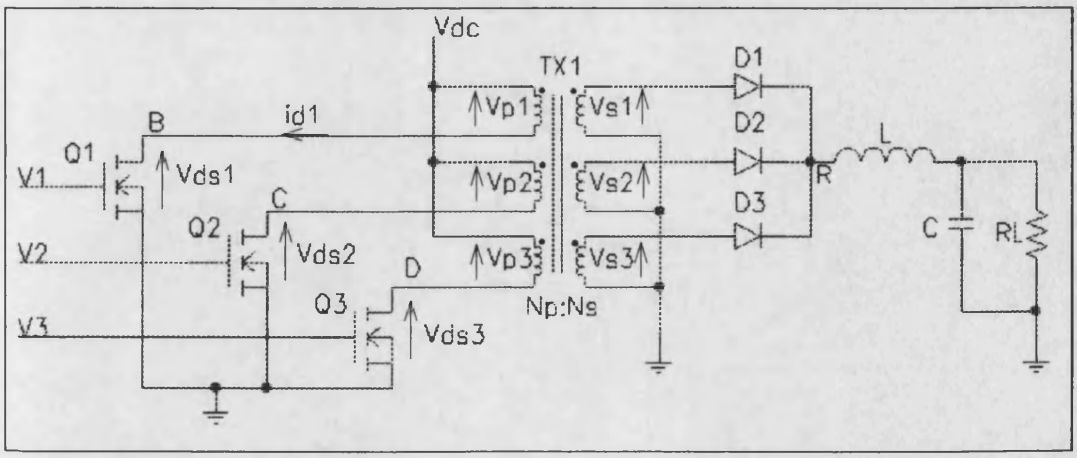

Fig. 5-3 The power section of the three-phase push-pull converter

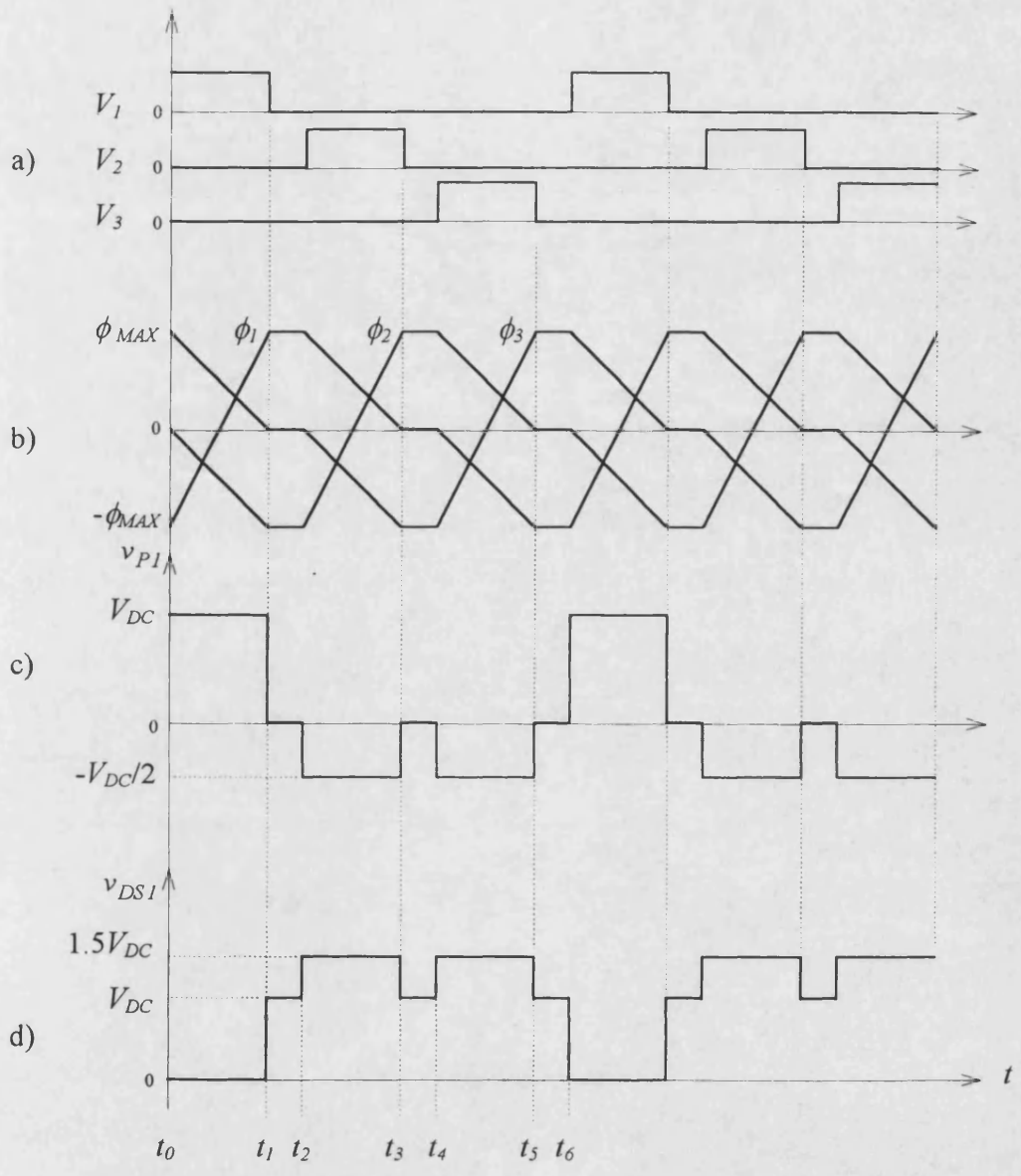

Fig. 5-4 Typical waveforms for the three-phase dc/dc push-pull converter a) control signals, b) the flux in each limb, c) the primary voltage, v_{P1}, and d) the switch voltage, V_{DS1}

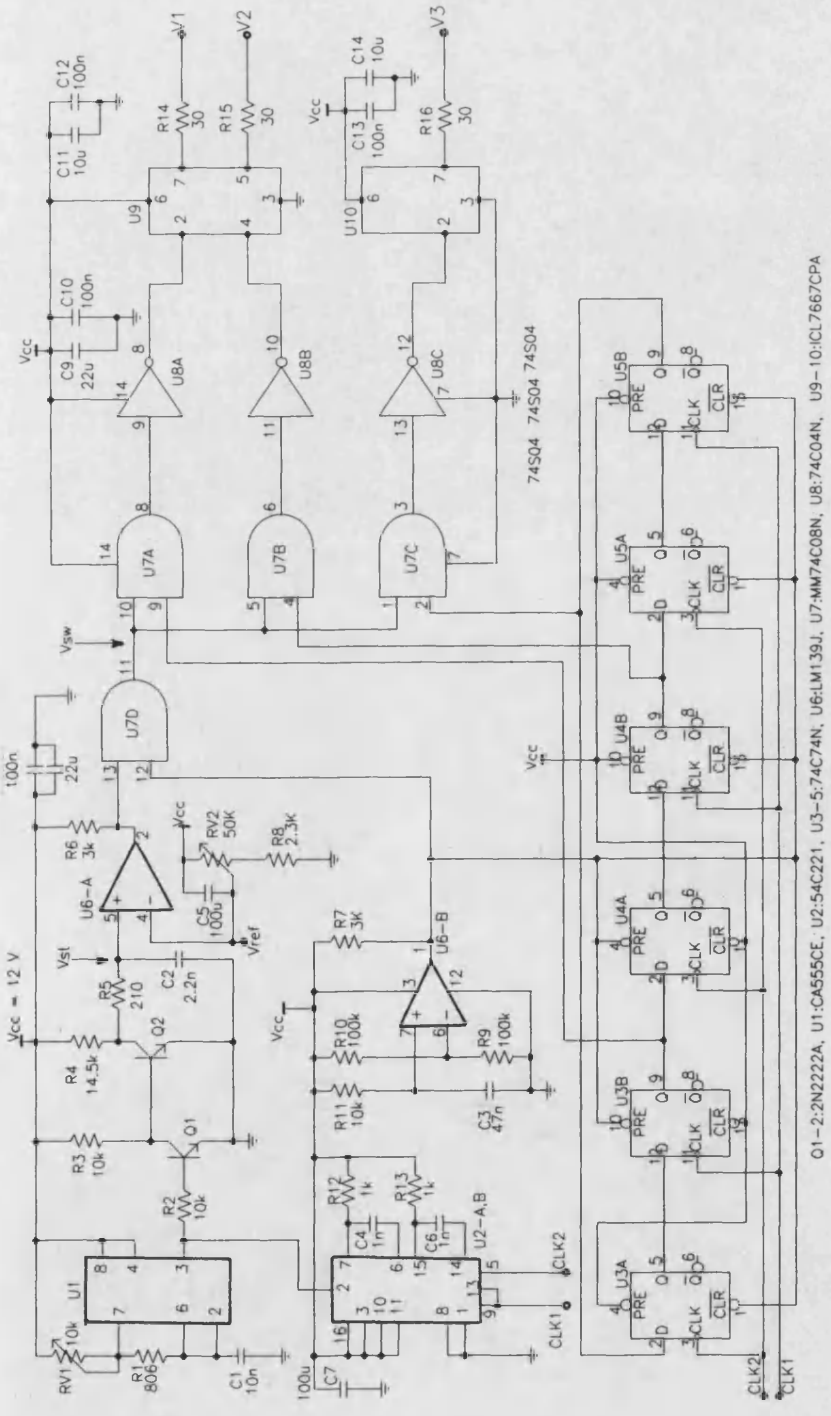

Fig. 5-5 The control circuit for the three-phase dc/dc push-pull converter

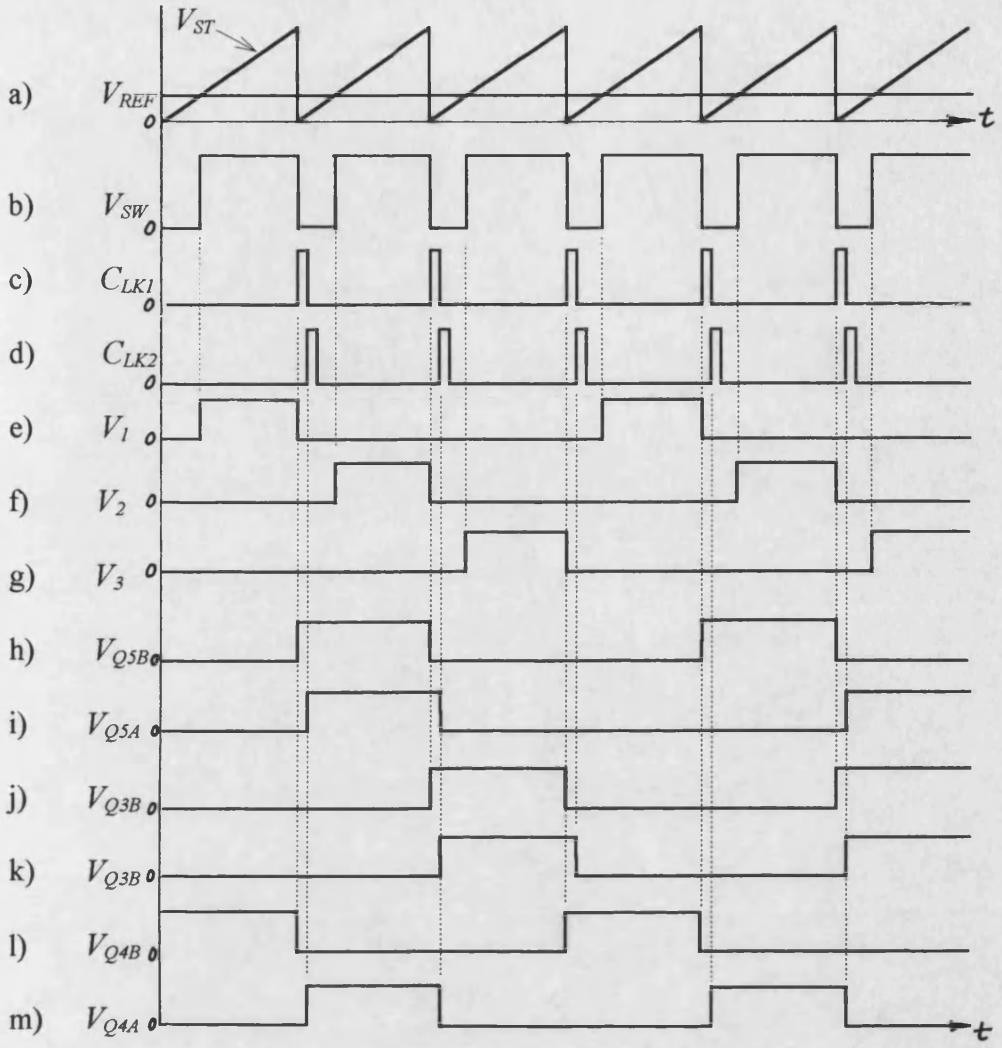

Fig. 5-6 Typical control signals for the control board

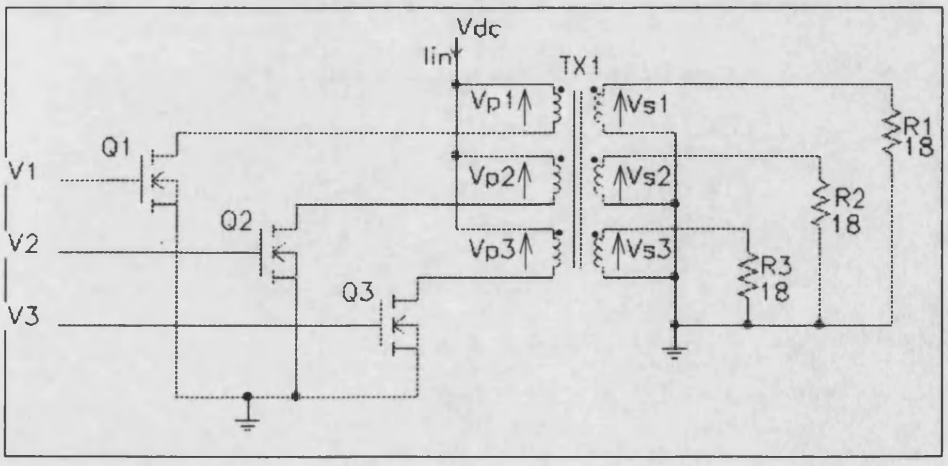

Fig. 5-7 A pure resistive-load three-phase push-pull converter

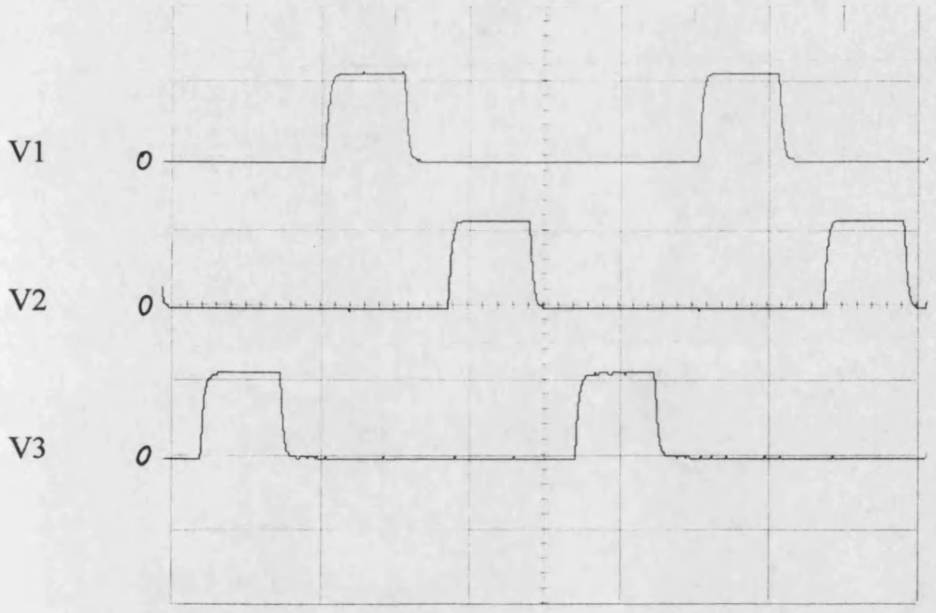

Fig. 5-8 The control signals: Ver.: 10V/div, Hor.: 10μs/div

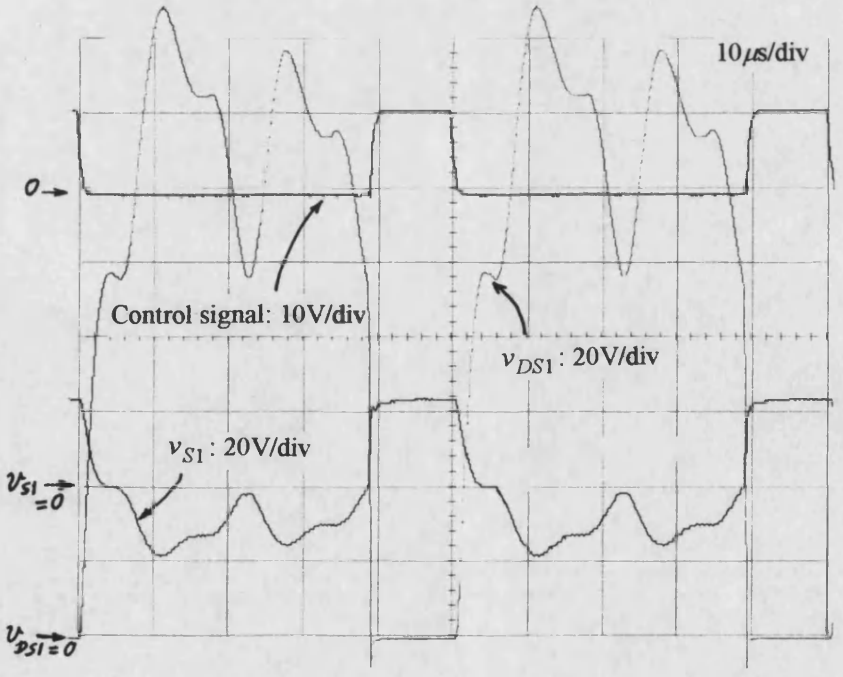

Fig. 5-9 Some practical waveforms of the three-phase dc/dc push-pull converter

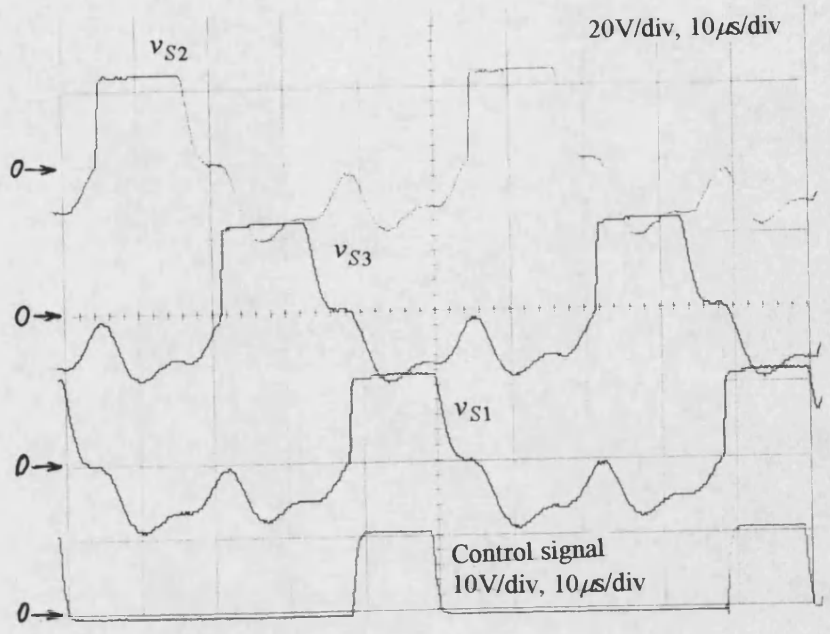

Fig. 5-10 Practical secondary voltages and one of the control signals

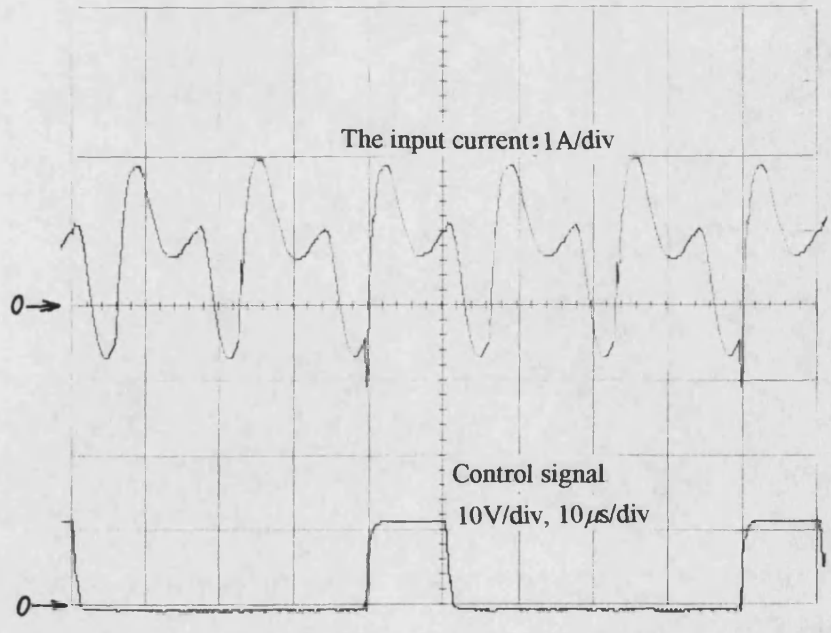

Fig. 5-11 The input current and one of the control signals

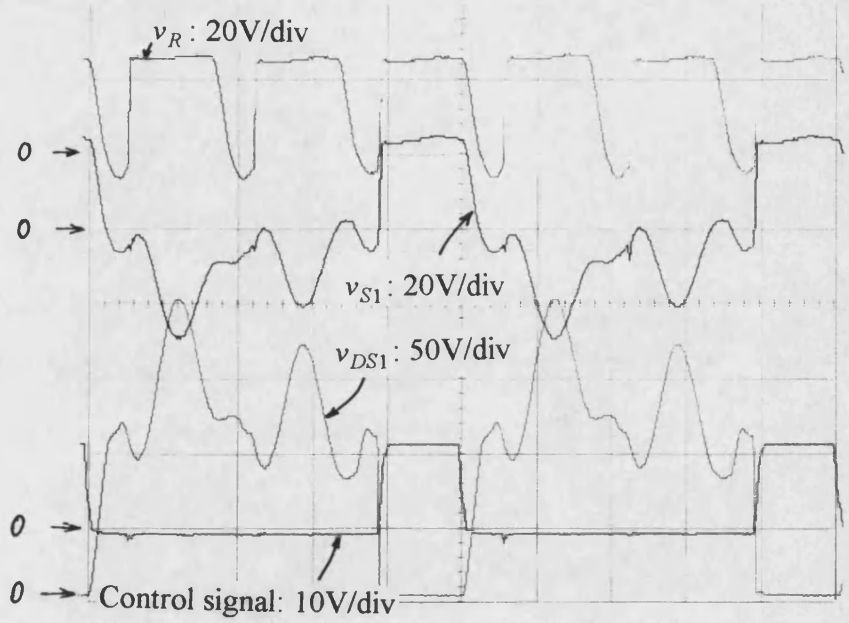

Fig. 5-12 Some other practical voltage waveforms of the three-phase dc/dc push-pull converter

LOW-FREQUENCY DC/AC INVERTERS USING HIGH-FREQUENCY TRANSFORMERS AND POWER DEVICES

6-1 INTRODUCTION

dc/ac inverters are widely used in un-interruptable power supplies and a.c. motor drives to generate a sinusoidal a.c. output at the required frequency. They are now commonly implemented using single- or three-phase voltage-source inverter bridges, comprising four or six transistors and freewheel diodes, which are controlled using sine-weighted PWM techniques [1-3]. Alternative inverter topologies and control methods also exist but are gradually being superseded by the voltage-source inverter as fast, more easily controlled, power semiconductor devices become available in higher and higher current and voltage ratings, e.g. MOSFETs, IGBTs, GTOs.

In the simplest systems, naturally-sampled PWM is generated as shown in Fig. 6-1a, where a sinusoidal signal (the control signal, f_O) at the required frequency is compared with a ramp or triangular signal (the carrier signal, f_{SW}) at a much higher frequency (preferably $f_{SW} / f_O >> 10$) to determine the switching pattern. The result is a constant frequency pulsed waveform in which the pulse widths are modulated by the low-frequency signal, as shown in Fig. 6-1b. If this signal is filtered by a low-pass filter, the high-frequency content will be very much attenuated, and the output waveform is approximately sinusoidal and phase-shifted due to the output low-pass filter, as shown in Fig. 6-1b.

In conventional low-frequency inverters, the transformer core flux varies sinusoidally as shown in Fig. 6-2a, and the transformer must be designed to operate at the low

output frequency, usually about 50/60 Hz or 400 Hz. Iron powder or laminated steel cores are, therefore, used for such applications. This low-frequency transformer adds significantly to the overall weight and volume of the inverter system.

However, if the core flux is forced to reset to zero at the end of each high-frequency switching cycle, f_{SW}, as shown in Fig. 6-2b, the transformer can now be designed for operation at the high switching frequency rather than at the low output frequency. Ferrite cores can, therefore, be used giving a much reduced transformer weight and size and, hence, cost [see Sec. (6-5)].

This technique has been applied in push-pull [4] and single-ended forward-converter [5-6] inverters. However, the methods of controlling the power devices and the core flux waveforms have not been clearly described. A study has, therefore, been conducted to apply this technique to the most commonly-used transformer-isolated power converter topologies. The principle of operation of each topology is first presented including the control method, followed by an estimation of the power device voltage and current ratings required. Conduction and switching power losses are evaluated for each topology over a wide f_{SW} range, and given to allow comparison of converter performance.

6-2 INVERTER TOPOLOGIES

This section presents the principle of operation of the main low-frequency inverters that use high-frequency transformers and devices, including the control method.

Fig's 6-3a, b and c show push-pull, half-bridge and full-bridge inverters that use low-frequency transformers, and Fig. 6-4 shows typical waveforms for operation with heavy output filtering and connection to a resistive load. Fig. 6-4a shows the low-frequency modulation and the high-frequency triangle signals which give the PWM waveform shown in Fig. 6-4b. This PWM waveform controls switch Q_1 in Fig. 6-3a, whereas a reverse version of it controls switch Q_2, as shown in Fig. 6-4c. The resulting transformer secondary voltage looks like that shown in Fig. 6-4d, which,

when averaged through the output filter, gives a similar waveform to that of the modulation signal, as shown in Fig. 6-4e. The variation in transformer core flux density looks like that shown in Fig. 6-4f. The fundamental component of the core-flux density is changing at the low output frequency. This requires that the transformer must be designed at this low frequency, which results in a high system weight and volume. Therefore, if no galvanic isolation is required, half- and full-bridge inverters may be used without transformers, as shown in Fig. 6-5, and considerable weight, size and cost savings will thereby be achieved.

The principles of operation of the low-frequency inverters are covered in [1-2] and are, therefore, not included here. However, the power losses and power devices voltage and current ratings for these and the high-frequency inverters are estimated.

6-2-1 High-frequency forward-converter inverters

Fig. 6-6a shows the power stage of a high-frequency single-ended forward-converter inverter, and Fig. 6-7 shows typical waveforms for this inverter.

It can be seen that the primary and reset circuits are identical to the normal forward converter. However, the secondary circuit comprises two secondary windings and associated rectifiers and freewheeling diodes, and two secondary power semiconductor switches which are shown as mechanical switches for clarity.

Switch Q_1 is controlled in the normal way by PWM pulses at high frequency, as shown in Fig. 6-7b. During the first positive half of the output low frequency, Q_2 is turned on. Positive PWM pulses are applied to the output filter similar to those shown in Fig. 6-7b. During the negative half of the output frequency, Q_3 is turned on and Q_2 is turned off. Negative PWM pulses are, therefore, applied to the output filter. As a result of this, a similar waveform to the modulating signal is obtained from the output of the filter which averages the positive and negative PWM pulses, as shown in Fig. 6-7c.

The transformer flux density varies as shown in Fig. 6-7d and is switched at high frequency as in the normal forward converters. Therefore, a much smaller transformer may be used. Switches Q_2 and Q_3 are referenced to ground and, hence, their driving circuit is very much simplified.

Fig. 6-6b shows a high-frequency double-ended forward-converter inverter which is controlled in the same way but uses two primary switches to reduce the voltage stress across the power switches.

6-2-2 High-frequency push-pull inverters

Fig. 6-8 shows the power stage of a push-pull inverter which uses a high-frequency transformer and Fig. 6-9 shows typical waveforms obtained using this inverter.
PWM pulses, Fig. 6-9b, are obtained in the normal way, as shown in Fig. 6-9a. Every other pulse of the PWM waveform controls one of the primary switches, as shown in Fig. 6-9c and d. Q_3 and Q_4 are controlled by a low-frequency signal as described in Sec. (6-2-1). The waveform at the input of the LC filter will be PWM pulses, as shown in Fig. 6-9e when Q_3 is "on" and Q_4 is "off". When Q_4 is "on" and Q_3 is "off", negative PWM pulses are obtained (not shown). Therefore, the output of the LC filter will be the average of these pulses, i.e. a sinusoidal low-frequency waveform if the modulating signal is sinusoidal. With this control method, the flux density returns to zero within each switching cycle, or period T_S, and increases in the opposite direction during the next switching cycle, as shown in Fig. 6-9g. Therefore, the transformer may be designed to operate at high frequency, thus considerably reducing the weight and volume of the inverter. Fig. 6-10 shows how driving pulses v_A and v_B in Fig. 6-9 may be generated in practice.

6-2-3 High-frequency bridge inverters

Fig. 6-11 shows half- and full-bridge inverters using high-frequency transformers. The same control method used in high-frequency push-pull inverters is also applied to these inverters.

6-2-4 Boost converter as a pre-regulator

A dc/dc boost pre-regulator may be added to any of the above dc/ac inverter topologies to provide the required input d.c. voltage. This has the advantages of

increasing and stabilising the d.c. supply voltage to the inverter, thus reducing the peak primary current and, therefore, reducing power losses, as will be described in Ch. 7.

6-3 CALCULATING PEAK PRIMARY CURRENTS IN DC/AC INVERTERS

6-3-1 Single- and double-ended forward-converter inverters

In forward converters, one transformer-drive voltage pulse is produced in each switching cycle. In inverters based on the forward converter, the widths of these pulses vary sinusoidally with the maximum pulse widths occurring at the peaks of the sinewave. The pulse widths also depend on the amplitude modulation depth, m_a, and have a maximum value of:

$$T_{ON(\max)} = m_a / f_{SW} \tag{6-1}$$

where $m_a = \hat{V}_M / \hat{V}_C$ is the amplitude modulation depth, $\hat{V}_M$ is the peak modulation signal amplitude and $\hat{V}_C$ is the peak carrier signal amplitude.

Assuming the efficiency of the inverter is η from the d.c. supply voltage, V_{DC}, to the final r.m.s. a.c. voltage, V_O, the input power may be written as:

$$P_{IN} = \frac{P_O}{\eta} \tag{6-2}$$

To deliver specific P_O, the maximum inverter transformer primary current will occur at minimum d.c. supply voltage, $V_{DC(min)}$. Therefore it should be calculated at this voltage to determine the minimum inverter switch current rating.

First, peak inverter transformer primary current will be determined as a function of

nominal V_{DC}, P_O and other inverter parameters. Because f_{SW} is normally far greater than the maximum modulating-signal frequency, f_O (i.e. f_{SW}/f_O >100), PWM pulse widths at any switching cycle within the modulating-signal period may be approximated by Eq. (6-3), if f_{SW} is assumed an integer multiple of f_O.

$$T_{ONk} = \frac{m_a}{f_{SW}} \sin \omega t_k \tag{6-3}$$

where $t_k = kT_S$ and $k = 1, 2, 3, \ldots, f_{SW} / f_O$

Initially, transformer magnetising current will be neglected and it will be assumed that the approximate primary current at any switching instant is given by:

$$i_P(t_k) = \hat{I}_P \sin(\omega t_k - \phi) \tag{6-4}$$

where $\hat{I}_P$ is the peak primary current and ϕ is the phase shift between the reference sinewave signal (the modulating waveform) and the primary current waveform.

The input energy delivered during any switching cycle to the output through the transformer, neglecting the voltage drop across the primary switches and assuming that the current is approximately constant during the turn-on time, is:

$$E_i(t_k) = \int_0^{T_{ONk}} vid\tau \tag{6-5a}$$

$$E_i(t_k) = V_{DC} i_P(t_k) T_{ONk} = V_{DC} \hat{I}_P \sin(\omega t_k - \phi) \frac{m_a}{f_{SW}} \sin \omega t_k$$

$$E_i(t_k) = \frac{V_{DC} \hat{I}_P m_a}{\omega} \sin(\omega t_k - \phi) \sin \omega t_k \frac{\omega}{f_{SW}}$$

$$E_i(t_k) = \frac{V_{DC} \hat{I}_P m_a}{\omega} \sin(\omega t_k - \phi) \sin \omega t_k \Delta\theta \tag{6-5b}$$

where $\Delta\theta = \frac{2\pi}{f_{SW} / f_O} = \frac{2\pi}{m_f}$ (6-6)

The input power is the average of Eq. (6-5b) over the output-frequency, f_O, half-cycle, as given by Eq. (6-7).

$$P_{IN} = 2f_O \sum_{k_\phi}^{k_\phi+\pi} \frac{V_{DC}\hat{I}_P m_a}{\omega} \sin(\omega t_k - \phi)\sin\omega t_k \Delta\theta$$

$$P_{IN} = \frac{1}{\pi} \sum_{k_\phi}^{k_\phi+\pi} V_{DC}\hat{I}_P m_a \sin(\omega t_k - \phi)\sin\omega t_k \Delta\theta \qquad (6\text{-}7)$$

where $k_\phi = \frac{\phi}{2\pi} m_f$ and $m_f = \frac{f_{SW}}{f_O}$.

If the switching frequency is much higher than the low output frequency, as it is the case in most applications, then the discrete form of Eq. (6-7) may be approximated to the continuous form of Eq. (6-8), which is obtained by letting $\Delta\theta$ reduce to zero.

$$P_{IN} = \frac{1}{\pi} \int_{\phi}^{\pi+\phi} V_{DC}\hat{I}_P m_a \sin(\theta - \phi)\sin\theta d\theta \qquad (6\text{-}8)$$

$$P_{IN} = \frac{1}{2} m_a V_{DC}\hat{I}_P \cos\phi \qquad (6\text{-}9)$$

Combining Eq's (6-2) and (6-9), and solving for $\hat{I}_P$, gives Eq. (6-10).

$$\hat{I}_P = \frac{2}{\eta \cdot m_a} \frac{P_O}{V_{DC}\cos\phi} \qquad (6\text{-}10)$$

Two other current components should also be added to the above calculated current; the first is the primary magnetising current; the second is the output filter ripple current as seen by the primary circuit. Both current components should be calculated at minimum d.c. input voltage.

Since power losses are calculated at minimum d.c. supply voltage, $V_{DC(min)}$, the peak magnetising current will also be estimated at this voltage, as given by Eq. (6-11).

$$\hat{I}_M = \frac{1}{L_M}\int_0^{T_{ON(max)}} v_P dt \approx \frac{1}{L_M}\left(V_{DC(min)} T_{ON(max)}\right) = \frac{m_a \cdot V_{DC(min)}}{L_M f_{SW}} \tag{6-11}$$

where L_M is the primary magnetising inductance, and f_{SW} is the switching frequency. This current component is assumed to be less than 5% of the primary r.m.s. current. The filter ripple current reflected to the primary may be estimated as follows:

$$\hat{I}_R = \frac{N_S}{N_P}\frac{1}{L_F}\int V_F dt \tag{6-12}$$

where L_F is the filter inductance value and V_F is the voltage difference between the inductor terminals. In fact, this voltage difference varies during the switching cycle and can not be easily calculated. Also this voltage changes with filter inductance and capacitance values as these define the phase lag between the filter input and output voltages. Assuming zero phase lag at the output frequency, and neglecting the voltage drop across the rectifier diode, the output voltage peak may be defined as:

$$\hat{V}_O = m_a V_{S(min)} \tag{6-13}$$

where $V_{S(min)}$ is the secondary pulse amplitude at minimum d.c. input voltage, $V_{DC(min)}$. Assuming constant filter input and output voltages during the switching cycle, the ripple current may be written as:

$$\hat{I}_R = \frac{N_S}{N_P}\frac{1}{L_F}\left(V_{S(min)} - m_a V_{S(min)}\right) T_{ON(max)}$$

$$\hat{I}_R = \frac{N_S}{N_P}\frac{V_{S(min)}}{L_F}(1-m_a) m_a \frac{1}{f_{SW}}$$

$$\hat{I}_R = \left(\frac{N_S}{N_P}\right)^2 \frac{V_{DC(min)}}{L_F f_{SW}} m_a (1-m_a) \tag{6-14}$$

Usually, this value is assumed to be less than 10% of the primary load current.

$$\hat{I}_M + \hat{I}_R = \frac{m_a \cdot V_{DC(\min)}}{L_M f_{SW}} + \left(\frac{N_S}{N_P}\right)^2 \frac{V_{DC(\min)}}{L_F f_{SW}} m_a (1 - m_a)$$

$$\hat{I}_M + \hat{I}_R = \frac{m_a \cdot V_{DC(\min)}}{f_{SW}} \left[\frac{1}{L_M} + \frac{N^2}{L_F}(1 - m_a)\right] \tag{6-15}$$

where $N = N_S / N_P$ is the transformer turns ratio.

To include the effect of $\hat{I}_M$ and $\hat{I}_R$ in determining the current rating of switches connected in the transformer primary circuit, a factor Δi will be used, whereby $\Delta i = (\hat{I}_M + \hat{I}_R) / \hat{I}_P$. This modifies the peak primary current as given by Eq. (6-16).

$$\hat{I}_P = (1 + \Delta i) \frac{2}{\eta \cdot m_a} \frac{P_O}{V_{DC(\min)} \cos\phi} \tag{6-16}$$

6-3-2 Half-bridge inverters

In half-bridge inverters, although half of the d.c. supply voltage is applied to the primary, the maximum transistor conduction duty-cycle is allowed to be double that in forward-converter inverters. Therefore, the peak primary current in half-bridge inverters, ignoring the ripple and magnetising currents, is the same as in forward-converter inverters, i.e.

$$\hat{I}_P = \frac{4}{\eta \cdot m_a} \frac{P_O}{V_{DC(\min)} \cos\phi} \tag{6-17}$$

where m_a in this topology is double that in forward-converter inverters, which gives the same peak current.

6-3-3 Push-pull and full-bridge inverters

In push-pull and full-bridge inverters, because the maximum transistor conduction duty-cycle and hence the maximum value of m_a is also allowed to be double that in forward-converter inverters, and the full d.c. supply voltage is applied to the transformer primary winding, the peak primary current to deliver the same output power will be half of that in the former two topologies, i.e.

$$\hat{I}_P = \frac{2}{\eta \cdot m_a} \frac{P_O}{V_{DC(\min)} \cos\phi} \tag{6-18}$$

where m_a is double that in forward-converter inverters, which gives half the peak current in the first two topologies.

6-3-4 Flyback inverters

Low-frequency flyback inverters using high-frequency transformers and devices have also been studied. It has been found that due to the principle of operation of flyback circuits, and because of the unavoidable phase shift between the output voltage and current due to the output filter capacitor, the current in the transformer secondary-winding will not reset properly when the output voltage is small or in opposite direction to the secondary current. A summary of this will now follow.

Fig. 6-12a shows the power stage of a flyback inverter using high-frequency transformer, Fig. 6-12b shows the fundamental components of the output voltage and the secondary current, and Fig. 6-12c shows the instantaneous secondary current. From Fig. 6-12b and c, Eq's (6-19) to (6-21) may be written, where T_R is the secondary current reset time, L_S is the secondary winding inductance, $\hat{i}_S$ is the peak secondary current at the end of each on-period and v_O is the output voltage.

$$\hat{i}_S = \hat{I}_S \sin\omega t \tag{6-19}$$

$$v_O = \hat{V}_O \sin(\omega t - \phi) \tag{6-20}$$

$$\frac{di_S}{dt} = \frac{v_O}{L_S} \Rightarrow \frac{\hat{i}_S}{T_R} = \frac{v_O}{L_S} \tag{6-21}$$

Therefore, a formula for T_R may now be written:

$$T_R = L_S \frac{\hat{I}_S \sin \omega t}{\hat{V}_O \sin(\omega t - \phi)} \tag{6-22}$$

If $\phi = 0$, $T_R = L_S \hat{I}_S / \hat{V}_O =$ constant, the secondary current is reset each switching cycle and the circuit operates in discontinuous conduction mode in the normal way. However, because the circuit has an output filter capacitor, the voltage always lags the current even with a purely resistive load. Therefore, when the voltage is zero, the current has a large value and it cannot reset against the small voltage. This case is worse when the voltage and current are in opposite directions. In this case, T_R is negative, i.e. the load filter capacitor becomes the source where the current flows from the capacitor to the inductor. This, of course, causes the transformer core to move into saturation.

The second problem with this technique is that when any of the secondary switches, Q_2 or Q_3, are turned on, the output voltage is not zero due to the phase shift. This causes a high current spike to flow in these switches and the associated secondary winding.

Some of design equations are included in App. (6) as a reference. These equations have been checked with PSPICE simulation results and found to agree very well.

The circuit in Fig. 6-13 was simulated using the design equations given in App. (6) and using two inductors, L_1 and L_2, rather than a transformer. Fig. 6-14 shows the output voltage and secondary currents at 20 kHz switching frequency. It can be seen that at the end of the first half of the low-frequency waveform (at 10 ms) when S_3 is turned on, the current is zero whereas, because of the phase shift between the voltage and the current, the voltage still has a high value. This causes a high current spike in the turned-on switch and the associated inductor due to this voltage.

Therefore, it seems that there is an inherent problem in using flyback circuits in dc/ac inverters because the output filter is effectively current fed rather than voltage fed as in all other transformer-isolated topologies.

6-4 SWITCH UTILISATION RATIO IN DC/AC INVERTERS

As described in [1], switch utilisation ratio may be given by Eq. (6-23), where V_O is the output r.m.s voltage, I_O is the output r.m.s. current, q is number of the power switches in the inverter, $\hat{V}_R$ is the maximum switch voltage stress and $\hat{I}_P$ is the maximum switch current, and assuming $m_a \leq 1$.

$$\text{Switch Utilisation Ratio, } SUR = \frac{V_O I_O}{q\hat{V}_R \hat{I}_P} \tag{6-23}$$

Since the maximum switch current, $\hat{I}_P$ was derived as a function of the output power, P_O, Eq. (6-24) will be used instead to define the switch utilisation ratio, *SUR*.

$$SUR = \frac{P_O}{q\hat{V}_R \hat{I}_P} \tag{6-24}$$

This will first be evaluated for low-frequency push-pull inverters, and then to all other topologies.

For low-frequency push-pull inverters, $q = 2$, $\hat{V}_R = 2V_{DC(\max)}$, $\hat{I}_P = \frac{2}{\eta m_a} \frac{P_O}{V_{DC(\min)} \cos\phi}$,

which gives:

$$SUR_1 = \frac{P_O}{2 \cdot 2V_{DC(\max)} \cdot \frac{2}{\eta m_a} \frac{P_O}{V_{DC(\min)} \cos\phi}} = \frac{\eta m_a \cos\phi}{8} \frac{V_{DC(\min)}}{V_{DC(\max)}} \tag{6-25}$$

Table (6-1) shows the power switch peak current, $\hat{I}_P$, the maximum switch voltage stress, $\hat{V}_R$, and the switch utilisation ratio, *SUR*, for all the inverter topologies previously described. Since the maximum value of m_a is 0.5 in both single- and double-ended forward-converter inverters, and 1 for all other topologies, a general formula was used to describe $\hat{I}_P$ and *SUR* using these two values.

As in dc/dc converters, push-pull and single-ended forward-converter inverters are not favoured for off-line applications due to the high reverse voltage which the power semiconductors must withstand, as can be seen in the $\hat{V}_R$ field in Table (6-1). With these circuits, an extra margin of about 30% of the calculated $2V_{DC(max)}$ should be added, which is represented by the Δv factor, to accommodate primary leakage-inductance voltage spikes.

It can be seen in row 11 of Table (6-1), that, where a boost converter is used as a pre-regulator to any of the previous topologies, the peak current is considerably reduced. In fact, the value of $V_{DC(min)}$ in the case of inverters designed to operate over the entire universal-input-voltage, i.e. (85-265)V a.c., is 120 V d.c.; whereas if a boost converter is used as a pre-regulator, this voltage will generally be above 375 V d.c. A reduction in the peak primary current of more than three times may, therefore, be achieved. The advantage of reduced inverter device cost and more efficient simpler design, because of the more tightly controlled inverter operating voltage and peak current, therefore, has to be weighed against the disadvantages of increased system complexity.

The lower *SUR* of the high-frequency dc/ac inverters shown in Table (6-1), largely, arises because extra switches are required to force bidirection magnetisation, or full reset, of the ferrite-cored transformers which must be reset during every switching cycle rather than during the output frequency period.

Table (6-1) alone is insufficient to make a judgement about the practicability of the high-frequency inverter systems. Other factors, such as inverter switching and conduction power losses and transformer volume and weight, must also be considered. Power losses have been separately studied in Ch. 7, whereas transformer volume and core estimation is considered next.

No	Topology	$\hat{I}_P$	$\hat{V}_R$	Absolute *SUR*	Switch No., q
1	L.F. Push-pull	$\hat{I}_{P1} = (1+\Delta i)\frac{2}{\eta}\frac{P_O}{V_{DC(\min)}\cos\phi}$	$(2+\Delta v)\ V_{DC(max)}$	$SUR_1 = \frac{\eta m_a \cos\phi}{8}\frac{V_{DC(\min)}}{V_{DC(\max)}}$	2
2	L.F. Half-Bridge	$2\hat{I}_{P1}$	$V_{DC(max)}$	SUR_1	2
3	L.F. Full-Bridge	$\hat{I}_{P1}$	$V_{DC(max)}$	SUR_1	4
4	H.F. S-E Forward	$2\hat{I}_{P1}$	$(2+\Delta v)\ V_{DC(max)}$	0.33 SUR_1	3
5	H.F. D-E Forward	$2\hat{I}_{P1}$	$V_{DC(max)}$	0.5 SUR_1	4
6	H.F. Push-Pull	$\hat{I}_{P1}$	$(2+\Delta v)\ V_{DC(max)}$	0.5 SUR_1	4
7	H.F. Half-Bridge	$2\hat{I}_{P1}$	$V_{DC(max)}$	0.5 SUR_1	4
8	H.F. Full-Bridge	$\hat{I}_{P1}$	$V_{DC(max)}$	0.75 SUR_1	6
9	L.F. Half-Bridge no transformer	$2\hat{I}_{P1}$	$V_{DC(max)}$	SUR_1	2
10	L.F. Full-Bridge no transformer	$\hat{I}_{P1}$	$V_{DC(max)}$	SUR_1	4
11	Boost + any of the above ten	Divide by 3.3	As before	Multiply by 3.3	+1

Table (6-1) Peak switch current, maximum voltage stress and *SUR* for dc/ac inverter topologies

6-5 Transformer-Core Volume and Weight Estimation

As mentioned earlier, transformers operating at high frequencies have smaller size and less weight compared to those operating at low frequencies. This section provides an estimation to the required transformer-core size in both low- and high-frequency dc/ac inverters, assuming the power transformed is constant.

The power which may be delivered through a transformer at any frequency can be given by Eq. (6-26) [7].

$$P = f_{SW} V_e \int_{B_L}^{B_H} H dB \tag{6-26}$$

where V_e is the effective transformer-core volume, f_{SW} is the switching frequency at which the transformer-core flux is changing, B_L is the minimum operating core-flux density, and B_H is the maximum operating core-flux density. Eq. (6-26) shows that the power delivered to the output is directly proportional to the switching frequency, effective core volume and the flux density excursion.

The term $\int_{B_L}^{B_H} H dB$ is simply the area enclosed by the operating hysteresis loop. This area cannot be easily evaluated because there is no single equation that describes the magnetic-field strength, H, as a function of magnetic-flux density, B. Therefore, core manufacturer's data sheets should be consulted to select the core size at specific power and switching frequency.

For example, Table (6-2) shows the volume and weight of three different core types chosen for transformers operating at 50, 400 and 20kHz, and transforming a power of 200W. It can be seen that as the switching frequency increases, smaller core volume and lower weight may be used. The relationship between the volume and the switching frequency is not linear as can be seen from Table (6-2). The reason for this is that the hysteresis loop area in high-frequency materials is much smaller; most notably, high-frequency ferrite materials must be operated at peak flux-densities which are at least 5 times smaller.

Core Type	Material	Output Power [W]	Switching Frequency [Hz]	Actual Volume [cm^3]	Weight [gr]
HWR 70/12 [2]	Laminated Steel	200	50	269.3	1190
HWR 10/24 [2]	Laminated Steel	200	400	132.6	577
ETD39 [3]	Ferrite N27	200	20k	19.9	60

Table (6-2) Volume and weight for different core types at 200W and different switching frequencies

As can be seen from Eq. (6-26), as the core-flux density excursion increases, the effective core volume may be reduced, i.e. a smaller core size may be selected. Conservative transformer designs using ferrite cores require flux density values not exceeding 200mT or even 160mT, to ensure that no saturation occurs under abnormal operating conditions. If measures are taken to detect the onset of transformer core saturation, then higher operating flux density excursion can be tolerated. This in turn, reduces the required core volume further. One of the methods used to detect transformer core saturation is to sense the transformer magnetising current, as discussed in detail in Ch. 4.

6-6 PSPICE SIMULATION OF HIGH-FREQUENCY DC/AC INVERTERS

Fig. 6-15 shows the schematic diagrams of the circuits used to simulate a high-frequency single-ended forward-converter inverter and a high-frequency half-bridge inverter. Fig. 6-16 shows the transformer core flux density in both circuits as obtained from PSPICE. It can be seen that the flux density in both circuits is changing at the high switching frequency, which enables the transformer to be designed to operate at that frequency.

Fig. 6-17 shows voltage and current waveforms obtained from the simulated forward-converter inverter, and Fig. 6-18 shows the same waveforms obtained from the simulated half-bridge inverter. It can be seen from waveform (a) in these two figures that the primary voltage of the half-bridge inverter is half that of the forward-converter inverter.

Because the half-bridge circuit is operating at double the amplitude modulation depth, m_a, the primary current peak has equal values in both circuits, as shown in waveform (c), and as was described in Sec's (6-3-1) and (6-3-2) and Table (6-1). To prove that the analysis in these sections is true, the same values used in simulation are used in Eq's (6-10) and (6-17) to evaluate the peak primary-current in both circuits. The parameters used are:

P_O = 146.4 W, $V_{DC(\min)}$ = 200 V, m_a = 0.95 in Eq.(6-17) and 0.475 in Eq. (6-10), $\cos\phi$ = 0.93, $\eta \approx 91\%$. The calculated peak primary-current is 3.64 A, whereas the simulated peak primary-current is 3.56 A, ignoring the ripple current in both cases. This shows a very good agreement between the analysis and the simulated results.

The primary current peaks and the duty cycle of the switches in both circuits vary sinusoidally, as described earlier. Waveforms (b) in both figures clearly show that the output voltage is sinusoidal and the filter input voltage is PWM pulses. The output voltage lags the fundamental of the filter input voltage due to the output capacitor.

CHAPTER SIX REFERENCES

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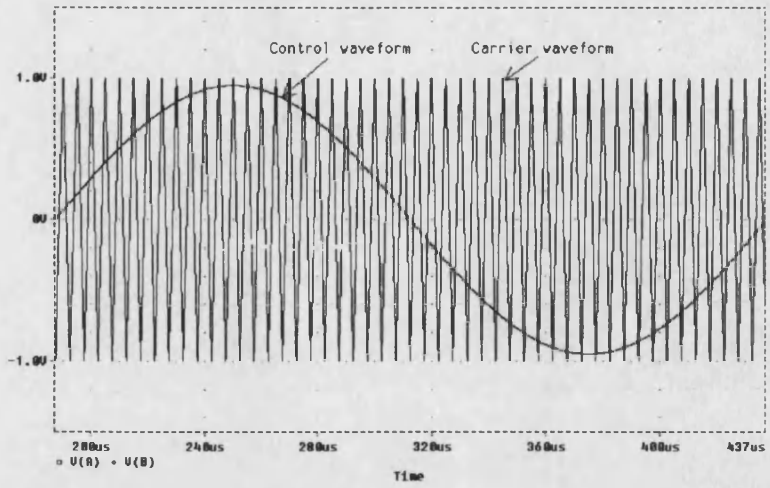
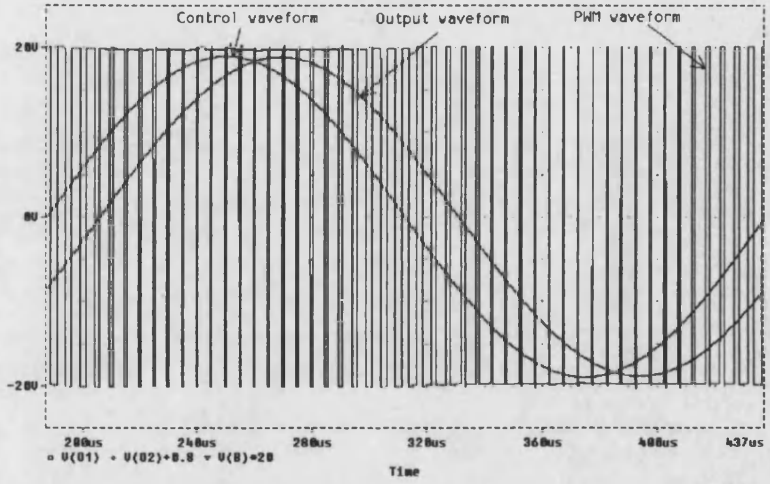
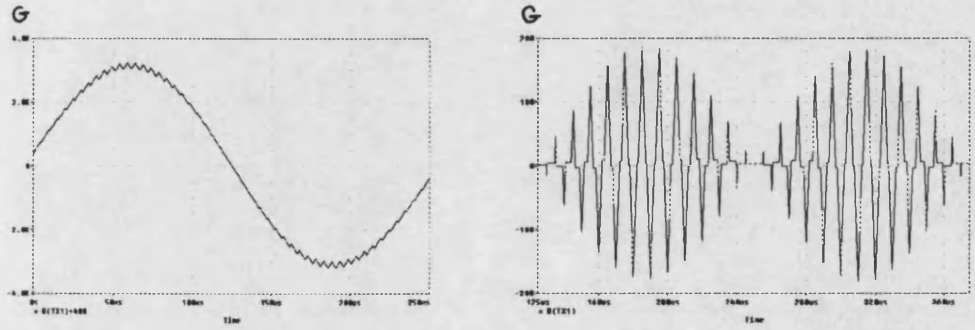


(a)



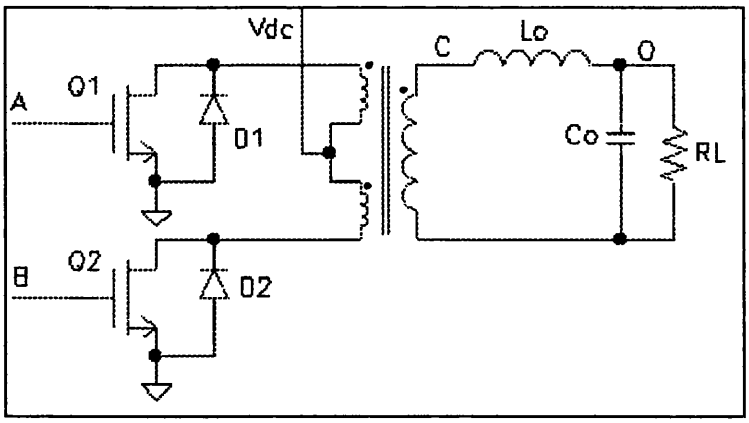
(b)

Fig. 6-1 Typical waveforms for a PWM dc/ac inverter



(a) (b)

Fig. 6-2 The transformer flux density waveform in a) low frequency and b) high frequency inverters



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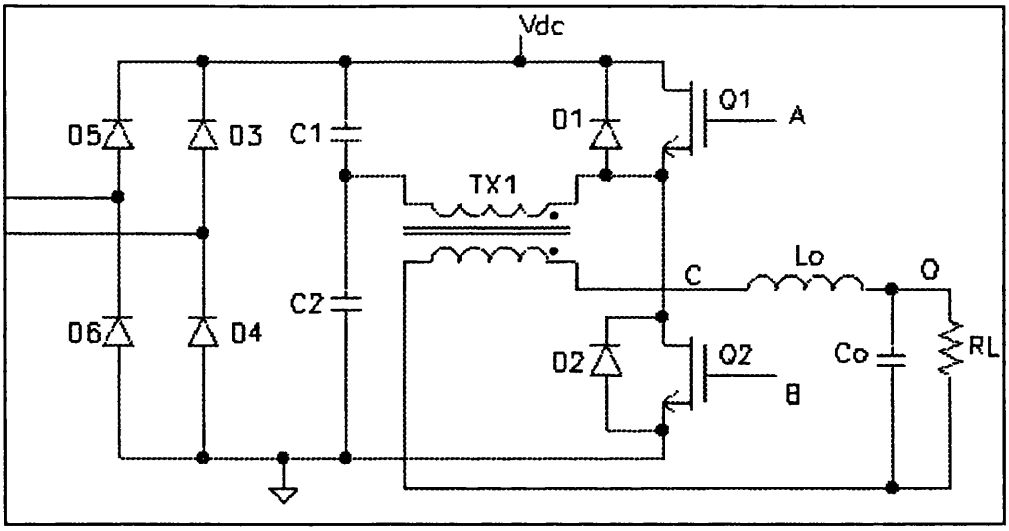

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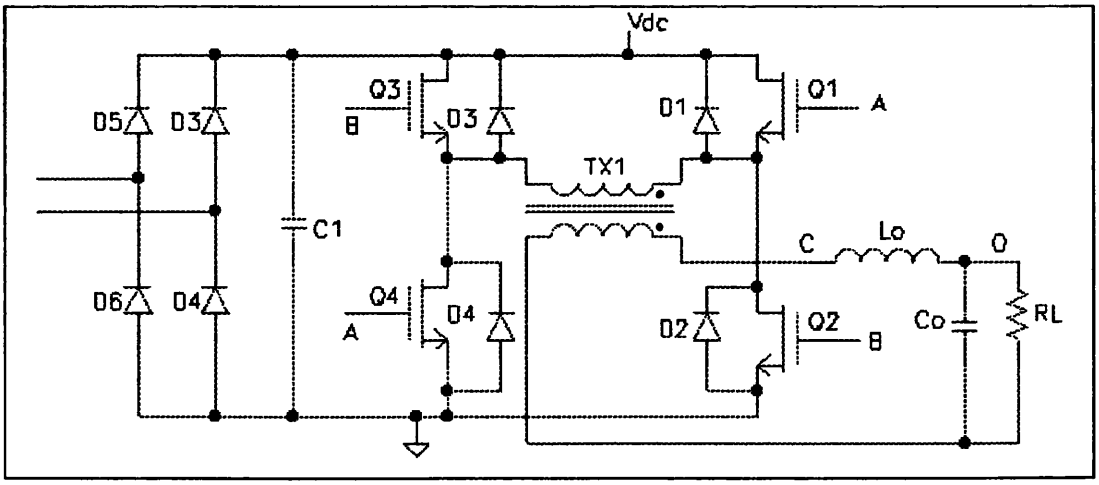


(c)

Fig. 6-3 Low frequency inverters a) push-pull, b) half-bridge and c) full-bridge

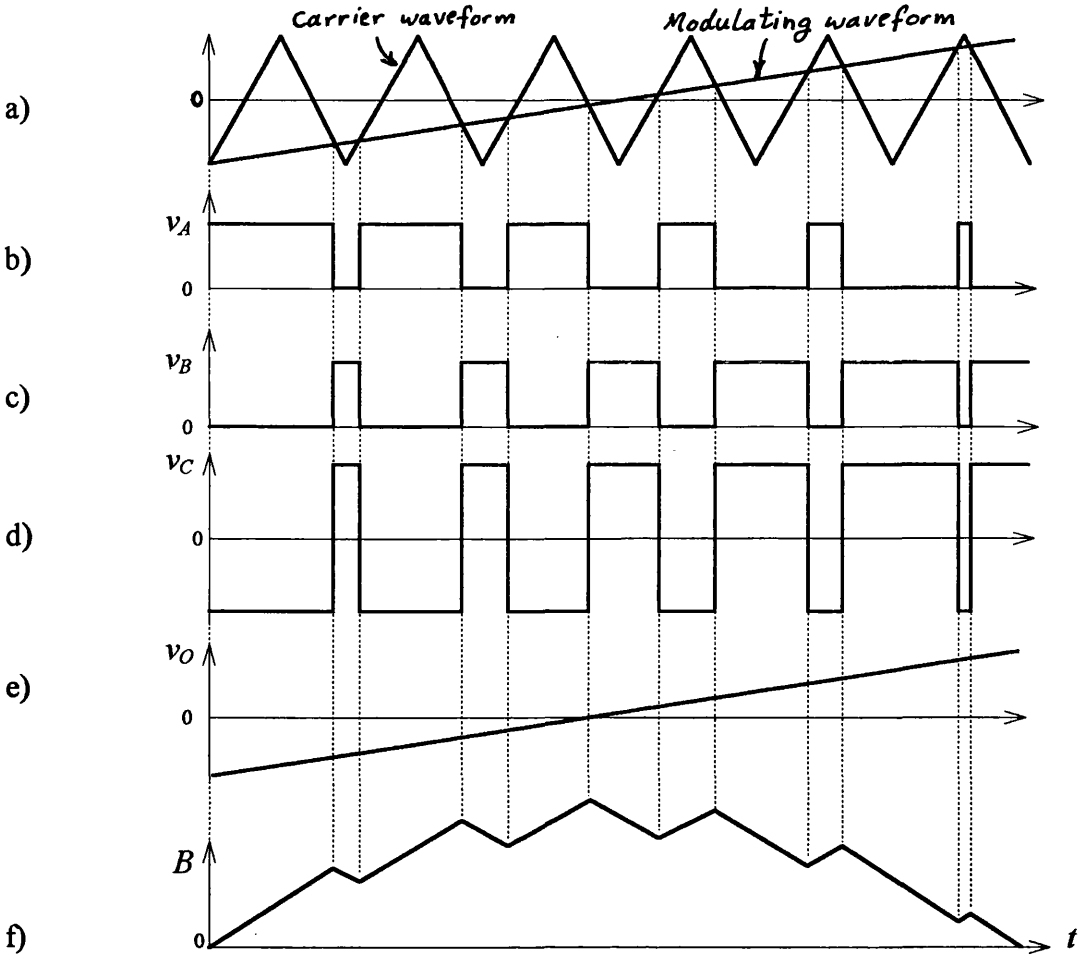


Fig. 6-4 Typical waveforms for low-frequency dc/ac inverters

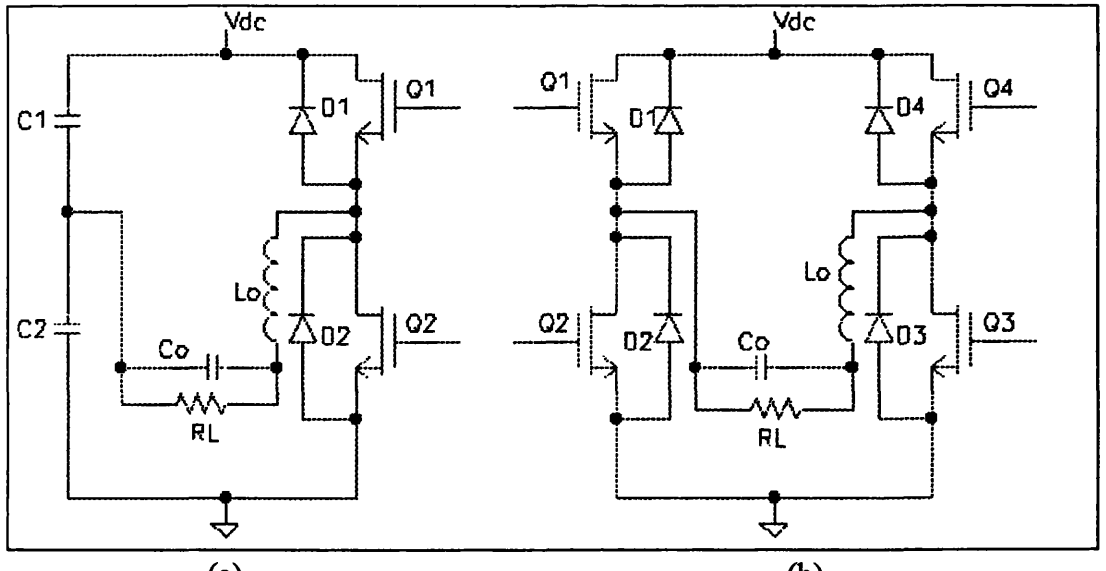
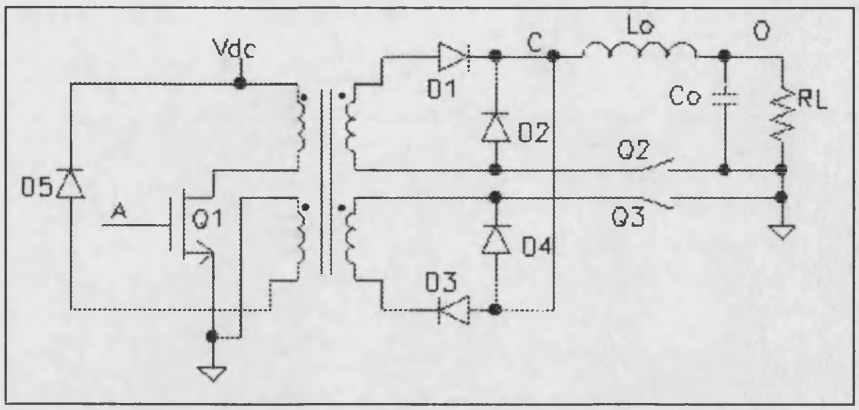
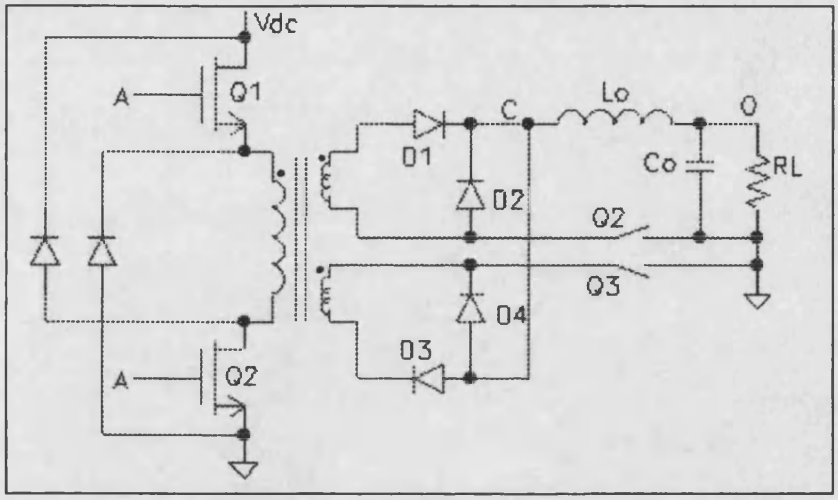


Fig. 6-5 Low-frequency inverters without transformers: a) half- and b) full-bridge



(a)



(b)

Fig. 6-6 The power stage of a) a high frequency single-ended and b) double-ended forward inverters

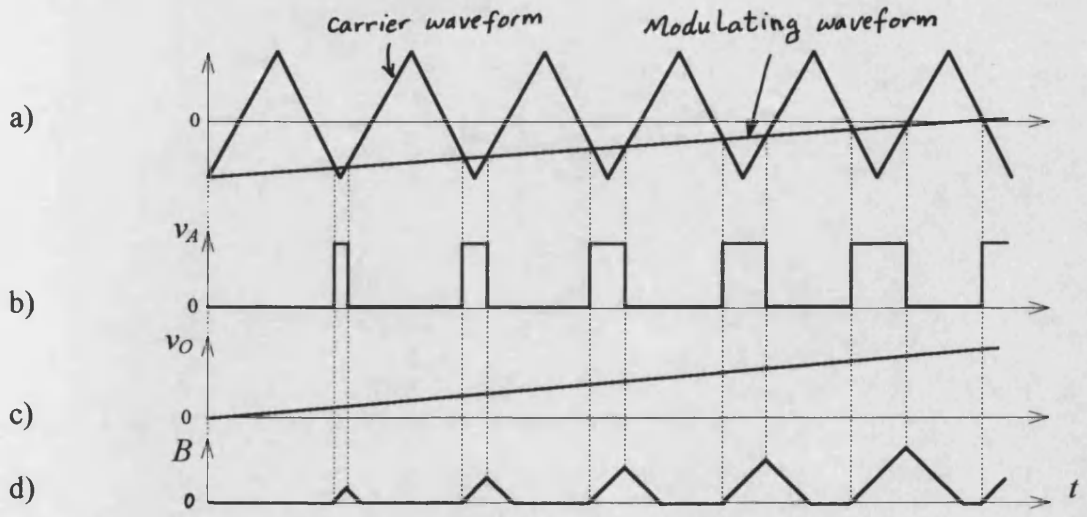


Fig. 6-7 Typical waveforms for high frequency forward inverters

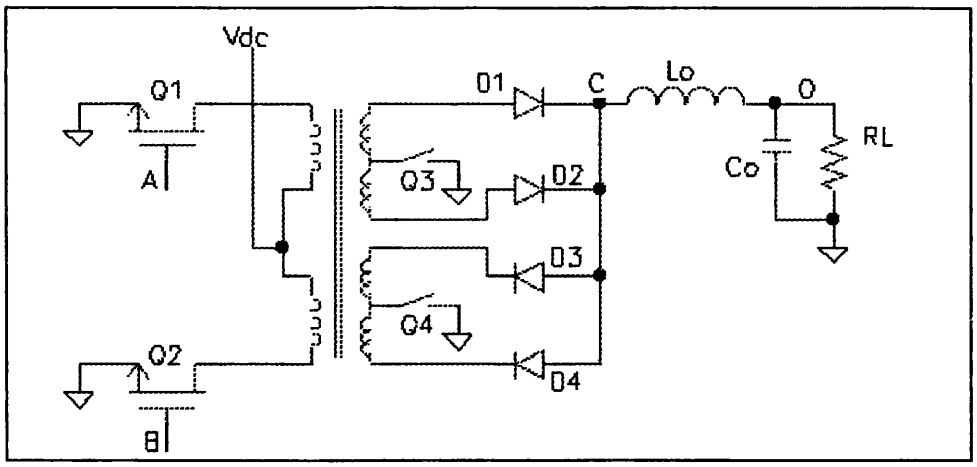


Fig. 6-8 The power stage of a high frequency push-pull inverter

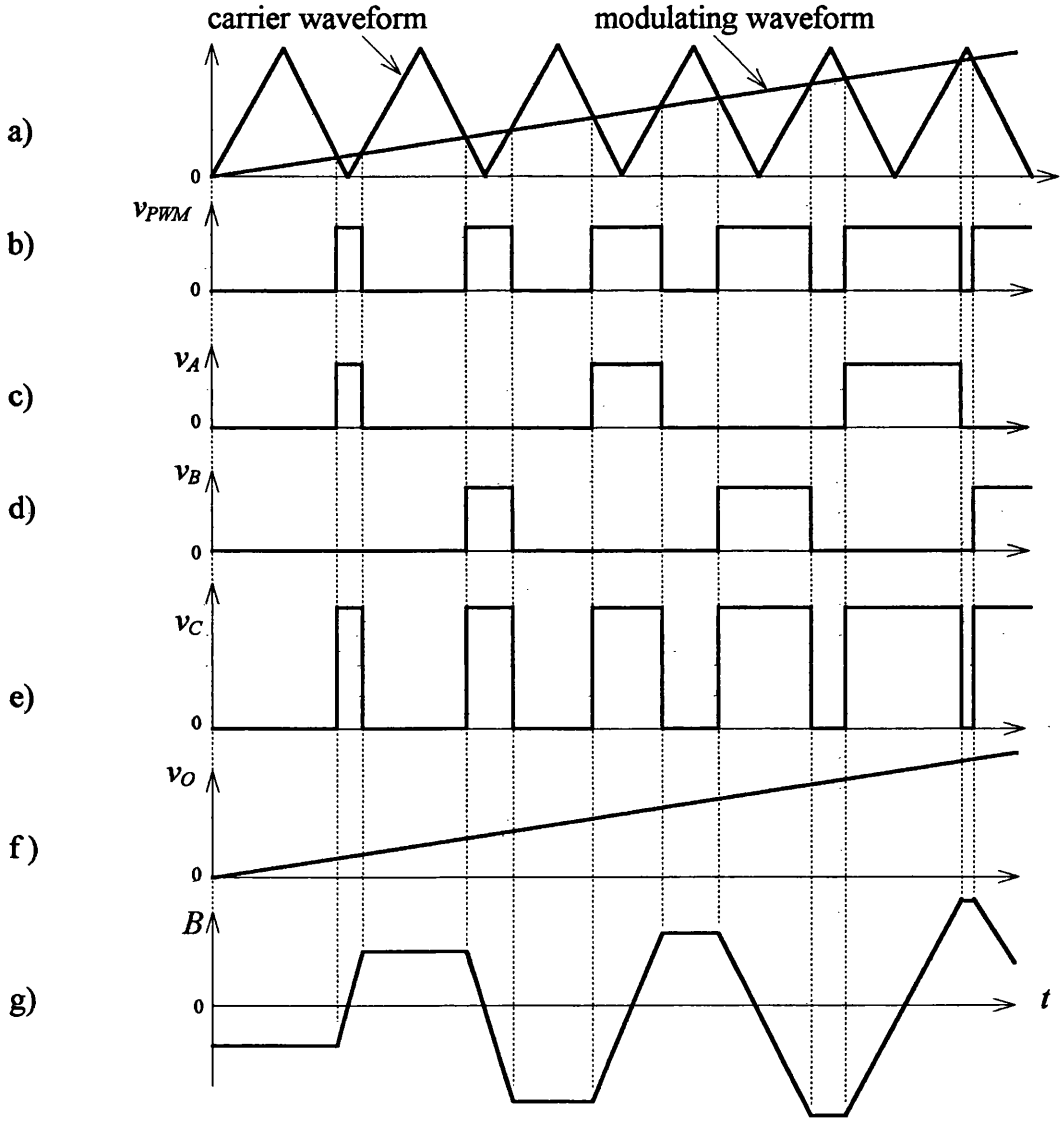
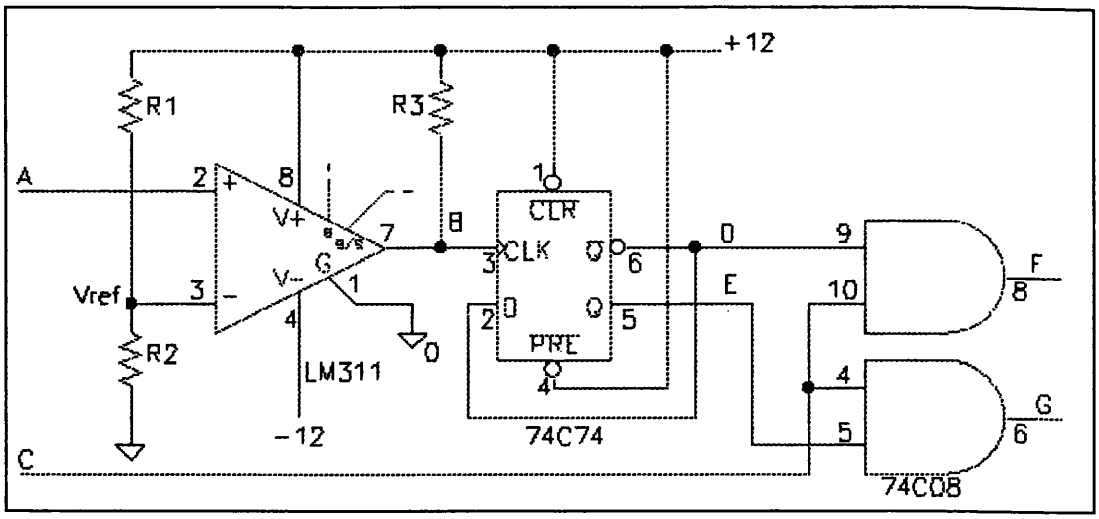
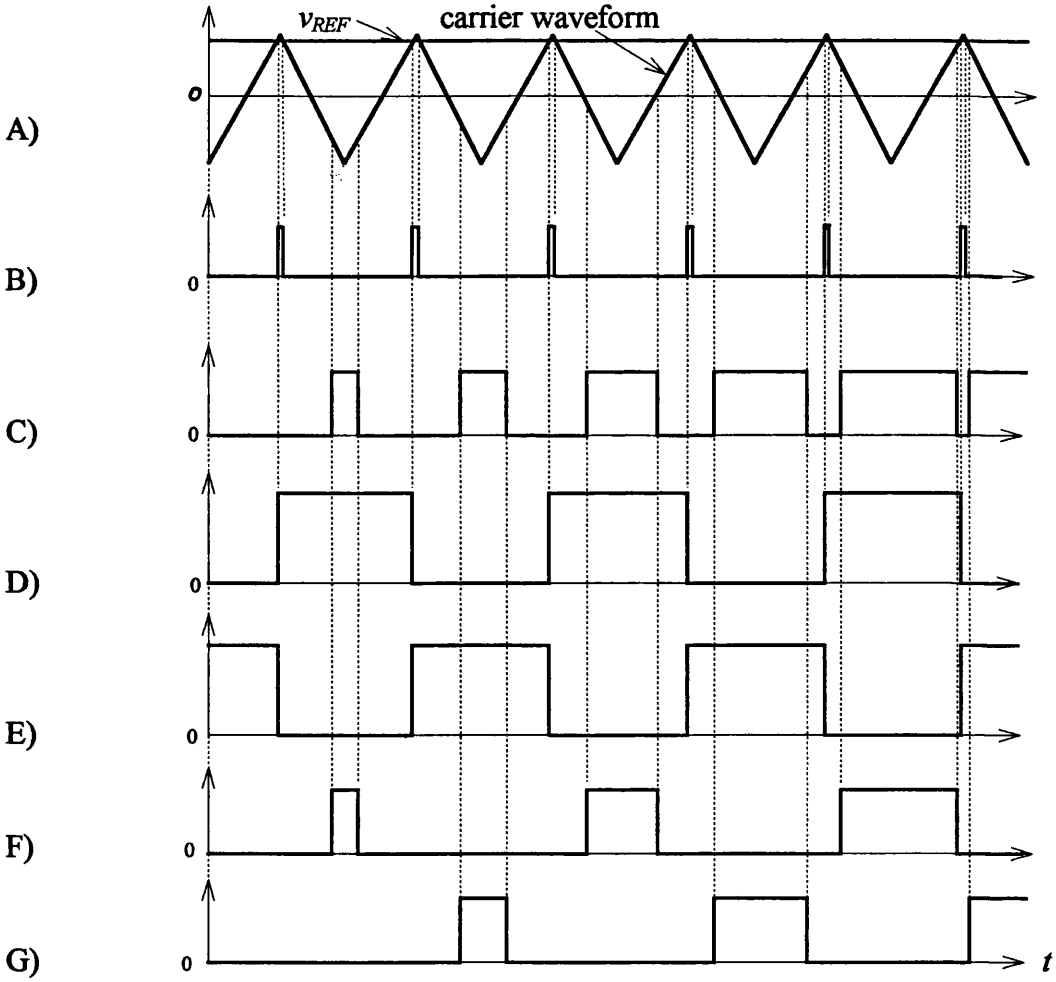


Fig. 6-9 Typical waveforms for high frequency push-pull, half- and full-bridge inverters

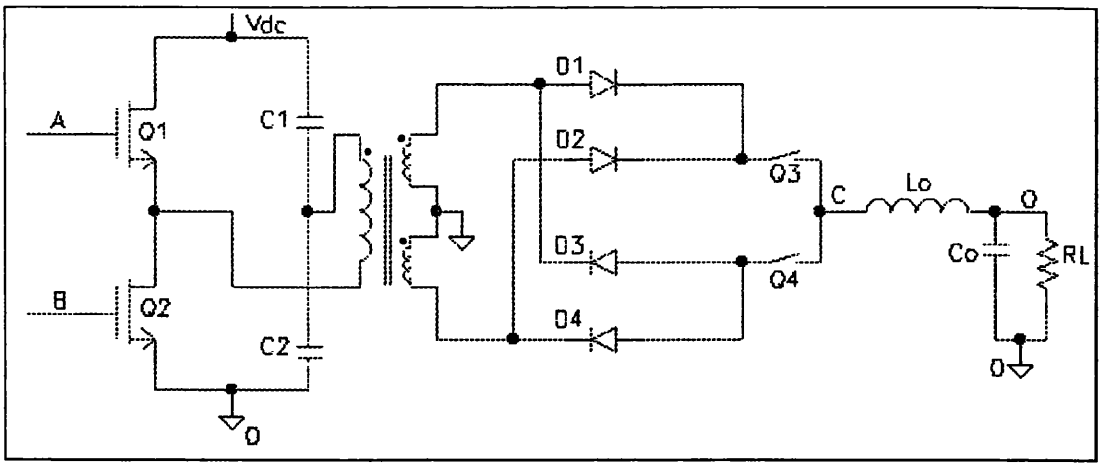


(a)



(b)

Fig. 6-10 a) A circuit to drive the power switches in push-pull, half- and full-bridge inverters and b) typical waveforms



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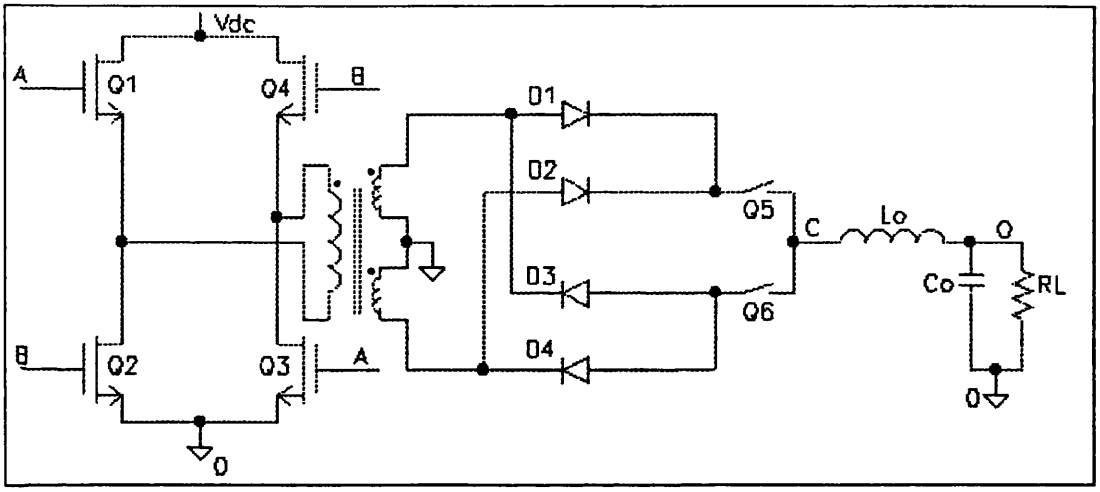
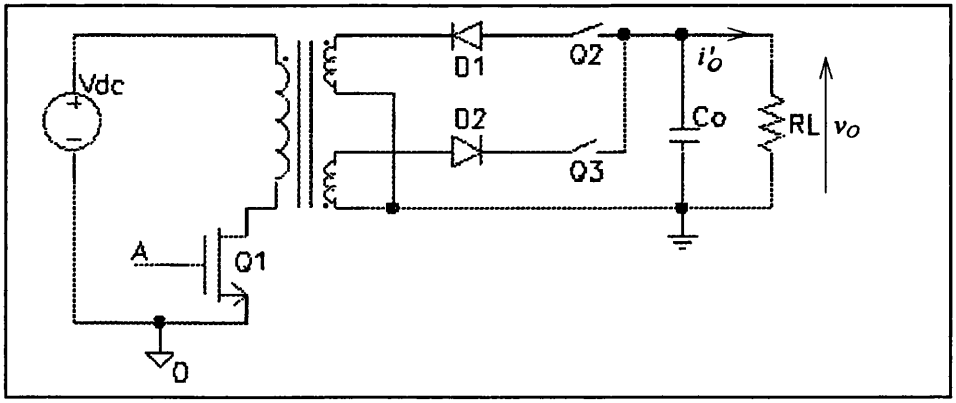


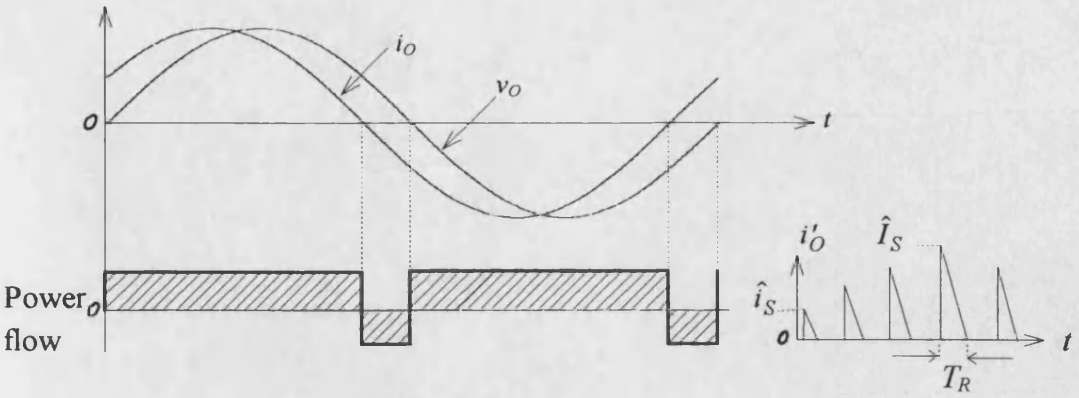
(b)

Fig. 6-11 High-frequency a) half- and b) full-bridge inverters



(a)

Fig. 6-12 a) The power stage of a high-frequency flyback inverter



(b) (c)

Fig. 6-12 b) required output waveform fundamental components, c) discontinuous i'_O waveform

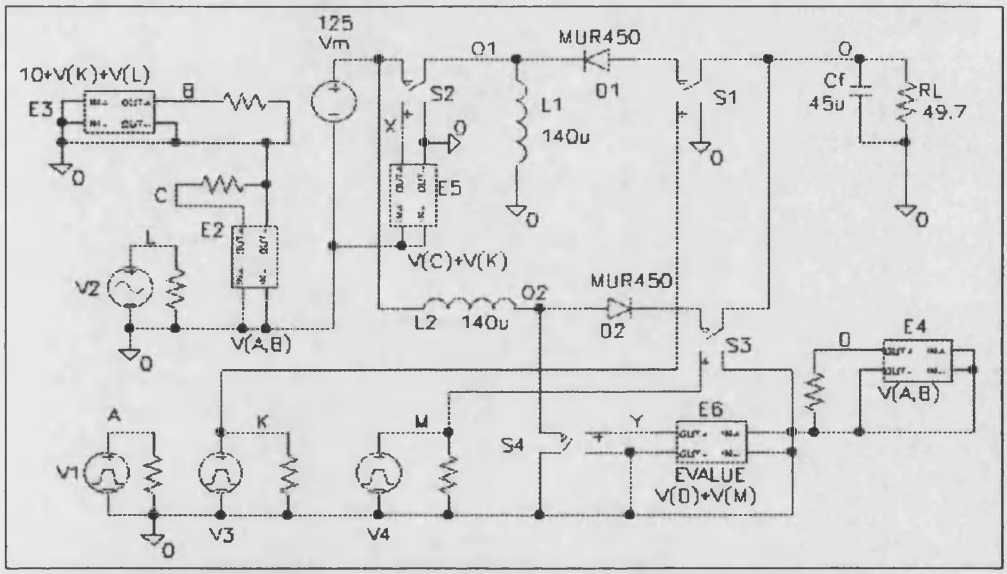


Fig. 6-13 The circuit used to simulate the flyback inverter

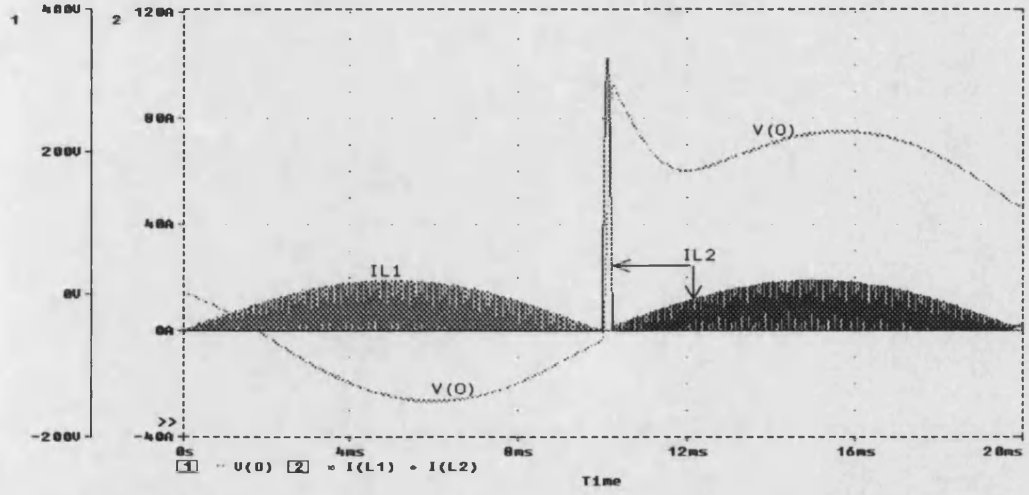
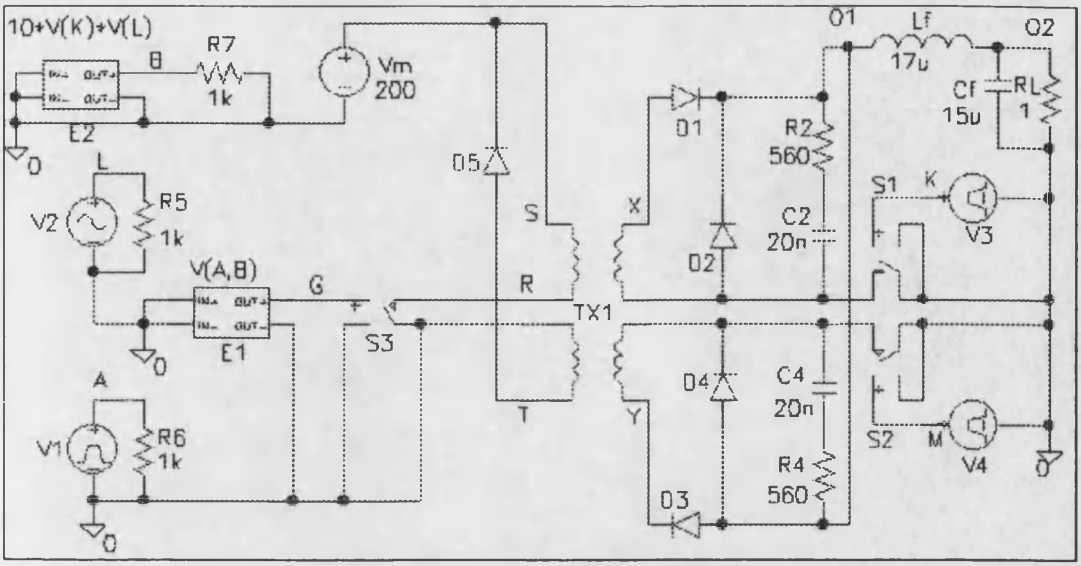


Fig. 6-14 Output voltage and current waveforms for flyback inverters



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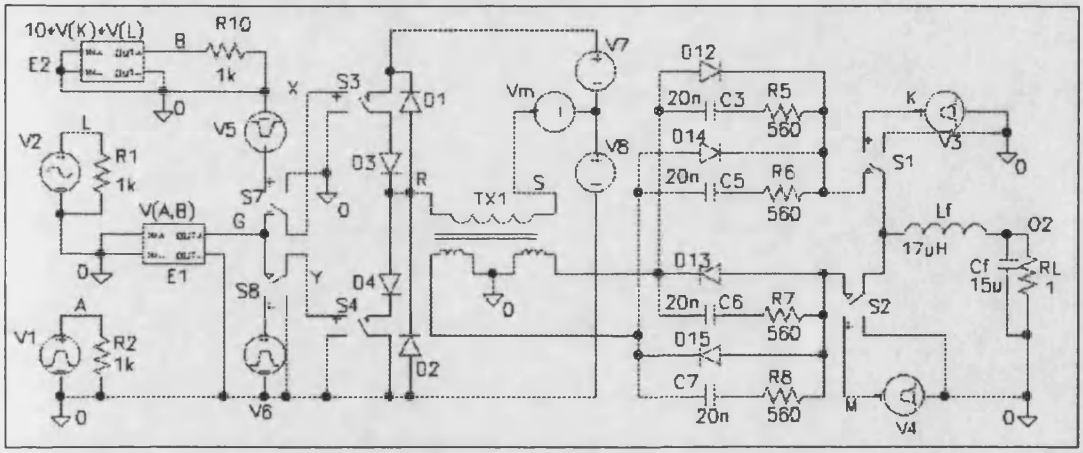
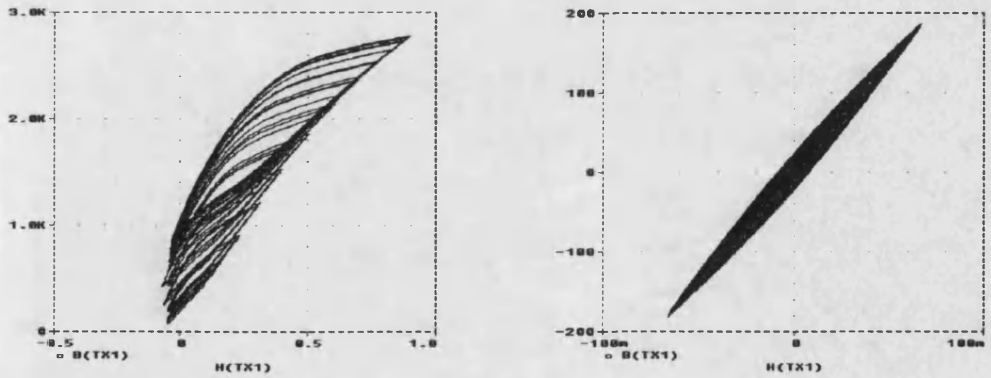


(b)

Fig. 6-15 The circuits used to simulate a) high frequency single-ended forward inverter and b) high frequency half-bridge inverter in PSPICE



(a) (b)

Fig. 6-16 The transformer core flux density in a) high frequency forward inverter and b) high frequency half-bridge inverter as obtained from PSPICE

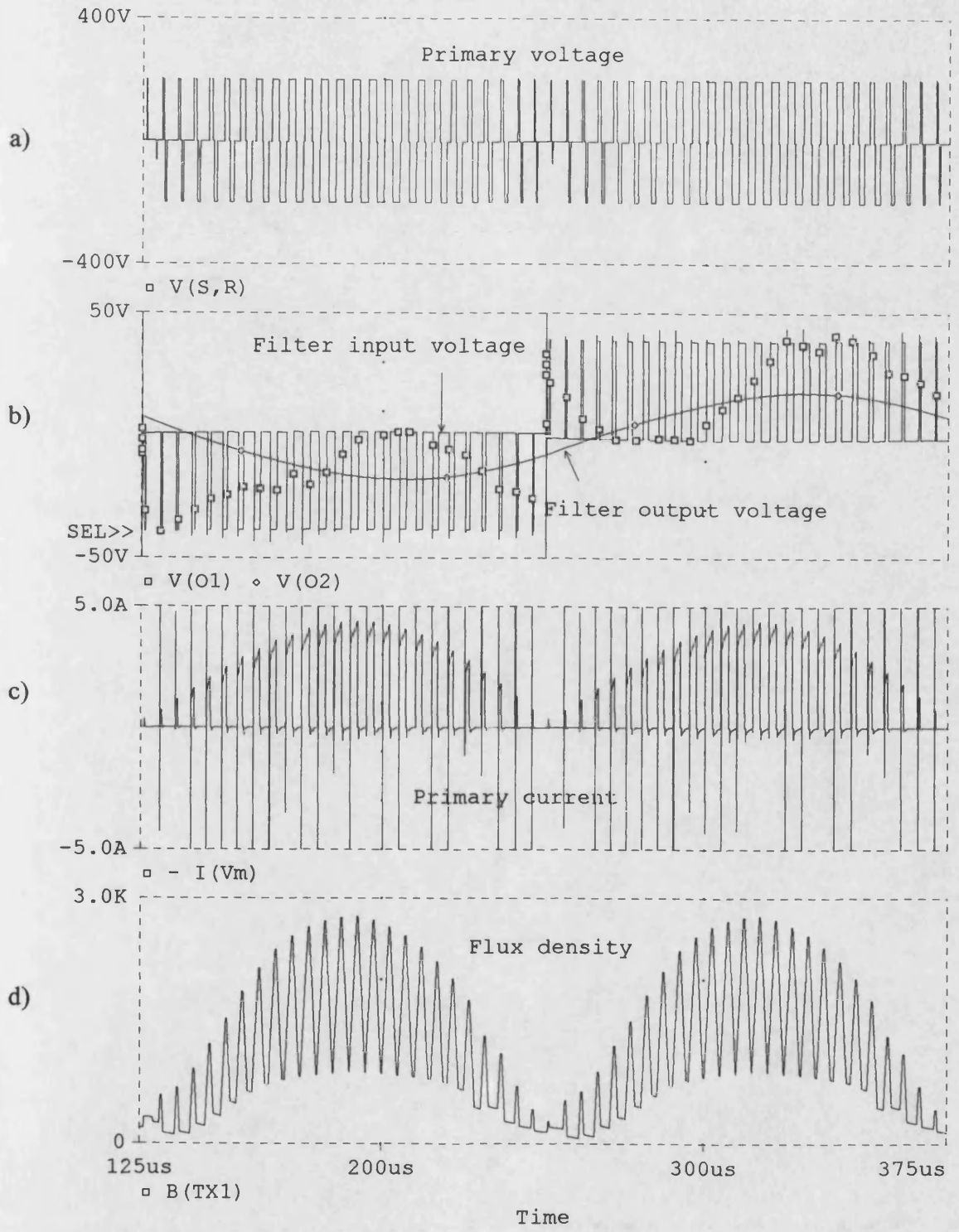


Fig. 6-17 Voltage and current waveforms for the high-frequency forward-converter inverter as obtained from PSPICE

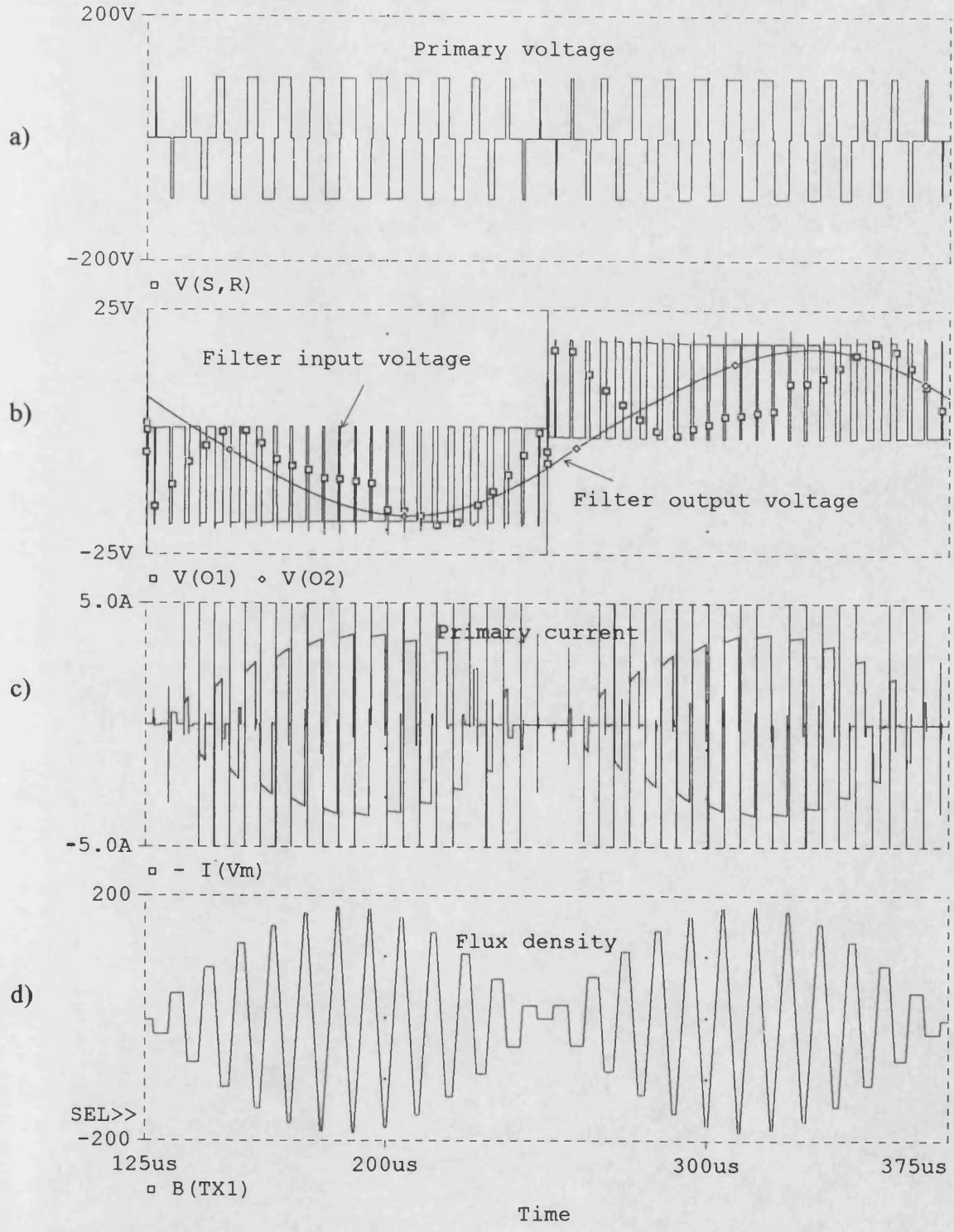


Fig. 6-18 Voltage and current waveforms for the high-frequency half-bridge inverter as obtained from PSPICE

POWER LOSSES IN DC/AC INVERTERS

7-1 CONDUCTION POWER LOSS CALCULATIONS

The voltage drop across any power semiconductor switch may be approximated by Eq. (7-1a), where V_{QO} is the power-switch on-state voltage drop and r_Q is the on-state resistance. The voltage drop across a power diode may be approximated by Eq. (7-1b) where V_{DO} is the diode threshold voltage and r_D is the dynamic resistance of the power diode.

$$v_Q(i) = V_{QO} + ir_Q \tag{7-1a}$$

$$v_D(i) = V_{DO} + ir_D \tag{7-1b}$$

The conduction power loss for each power switch and diode may then be estimated by Eq's (7-2a) and (7-2b).

$$P_{Q(con)} = \frac{1}{T}\int_0^T \left(V_{QO}i + r_Q i^2\right)dt \tag{7-2a}$$

$$P_{D(con)} = \frac{1}{T}\int_0^T \left(V_{DO}i + r_D i^2\right)dt \tag{7-2b}$$

However, in pulse-width-modulated systems, such as dc/ac inverters, the current as well as the conduction period of the power switches and diodes is pulse-width-modulated, and the discrete form of Eq's (7-2a) and (7-2b) should be used instead as shown in the general form in Eq's (7-3a) and (7-3b), where $\Delta\theta_Q$ and $\Delta\theta_D$ are the conduction angles of the switch and diode, respectively [1], and ϕ is the phase shift between the output voltage and output current.

$$P_{Q(con)} = \frac{1}{2\pi} \sum_{\phi/\Delta\theta}^{(\phi+2\pi)/\Delta\theta} \left[V_{QO}\hat{I}_P \sin(\theta-\phi) + r_Q \hat{I}_P{}^2 \sin^2(\theta-\phi) \right] \Delta\theta_Q \tag{7-3a}$$

$$P_{D(con)} = \frac{1}{2\pi} \sum_{\phi/\Delta\theta}^{(\phi+2\pi)/\Delta\theta} \left[V_{DO}\hat{I}_P \sin(\theta-\phi) + r_D \hat{I}_P{}^2 \sin^2(\theta-\phi) \right] \Delta\theta_D \tag{7-3b}$$

However, the conduction periods, or angles, of the power devices vary for each inverter topology, and will now be considered separately.

7-1-1 Low-frequency push-pull inverters

$$\Delta\theta_Q = \frac{1}{2}(1 + m_a \sin\theta)\Delta\theta \tag{7-4a}$$

$$\Delta\theta_D = \frac{1}{2}(1 - m_a \sin\theta)\Delta\theta \tag{7-4b}$$

Substituting Eq's (7-4a) and (7-4b) into Eq's (7-3a) and (7-3b), and reducing $\Delta\theta$ to zero, gives Eq's (7-5a) and (7-5b).

$$P_{Q(con)} \approx \frac{1}{2\pi} \int_{\phi}^{\phi+\pi} \left[V_{QO}\hat{I}_P \sin(\theta-\phi) + r_Q \hat{I}_P{}^2 \sin^2(\theta-\phi) \right] \left(\frac{1 + m_a \sin\theta}{2} \right) d\theta \tag{7-5a}$$

$$P_{D(con)} \approx \frac{1}{2\pi} \int_{\phi}^{\phi+\pi} \left[V_{DO}\hat{I}_P \sin(\theta-\phi) + r_D \hat{I}_P{}^2 \sin^2(\theta-\phi) \right] \left(\frac{1 - m_a \sin\theta}{2} \right) d\theta \tag{7-5b}$$

Solving Eq's (7-5a) and (7-5b) gives:

$$P_{Q(con)} \approx \frac{\hat{I}_P V_{QO}}{2}\left(\frac{1}{\pi}+\frac{m_a}{4}\cos\phi\right)+r_Q\hat{I}_P{}^2\left(\frac{1}{8}+\frac{m_a}{3\pi}\cos\phi\right) \quad (7\text{-}6a)$$

$$P_{D(con)} \approx \frac{\hat{I}_P V_{DO}}{2}\left(\frac{1}{\pi}-\frac{m_a}{4}\cos\phi\right)+r_D\hat{I}_P{}^2\left(\frac{1}{8}-\frac{m_a}{3\pi}\cos\phi\right) \quad (7\text{-}6b)$$

Because two switches and two diodes are active in one low-frequency cycle, the above two conduction power loss terms should be multiplied by 2 to give the total conduction losses in push-pull inverters using low-frequency transformers as shown in Eq's (7-7a) and (7-7b).

$$P_{Q(con)} \approx \hat{I}_P V_{QO}\left(\frac{1}{\pi}+\frac{m_a}{4}\cos\phi\right)+2r_Q\hat{I}_P{}^2\left(\frac{1}{8}+\frac{m_a}{3\pi}\cos\phi\right) \quad (7\text{-}7a)$$

$$P_{D(con)} = \hat{I}_P V_{DO}\left(\frac{1}{\pi}-\frac{m_a}{4}\cos\phi\right)+2r_D\hat{I}_P{}^2\left(\frac{1}{8}-\frac{m_a}{3\pi}\cos\phi\right) \quad (7\text{-}7b)$$

7-1-2 Low-frequency half-bridge inverters

In half-bridge inverters that use low frequency transformers, Eq's (7-7a) and (7-7b) are also applied to obtain switch and diode conduction losses. However, in this topology, the primary current is double that in push-pull inverters for the same output power, and this increases the conduction losses.

7-1-3 Low-frequency full-bridge inverters

Eq's (7-7a) and (7-7b) still apply for full-bridge inverters. However, because four switches and four diodes are active in one complete low-frequency cycle, the above two equations should be multiplied by 2, i.e.

$$P_{D(con)} = 2\hat{I}_P V_{QO}\left(\frac{1}{\pi}+\frac{m_a}{4}\cos\phi\right)+4r_Q\hat{I}_P{}^2\left(\frac{1}{8}+\frac{m_a}{3\pi}\cos\phi\right) \quad (7\text{-}8a)$$

$$P_{D(con)} = 2\hat{I}_P V_{DO}\left(\frac{1}{\pi}-\frac{m_a}{4}\cos\phi\right)+4r_D\hat{I}_P{}^2\left(\frac{1}{8}-\frac{m_a}{3\pi}\cos\phi\right) \quad (7\text{-}8b)$$

7-1-4 High-frequency single-ended forward-converter inverters

In single-ended forward-converter inverters using high-frequency transformers (see Fig. 6-6a), the conduction period of the primary power switch, $\Delta\theta_Q$, is the same as that for the rectifier diode, D_1 or D_3, as shown in Eq's (7-9a) and (7-9b). Freewheeling diodes, D_2 or D_4, conduct during the rest of the switching cycle, as given by Eq. (7-9c).

$$\Delta\theta_Q = m_a \sin\theta\Delta\theta \tag{7-9a}$$

$$\Delta\theta_{D1} = m_a \sin\theta\Delta\theta \tag{7-9b}$$

$$\Delta\theta_{D2} = (1 - m_a \sin\theta)\Delta\theta \tag{7-9c}$$

During the conduction period, the switch conducts the primary current, i_P, and D_1 conducts the secondary current, i_P/N. During the "off" period of the switch, D_2 conducts a current of i_P/N. These current values should be used to calculate conduction losses as will be described in the next sections.

Each of the secondary-side power switches conducts the secondary current for the complete low-frequency half-cycle.

In the subsequent sections Q_P refers to primary-side power switches and Q_S refers to secondary-side power switches.

7-1-4-1 Switch conduction loss

Because primary current waveforms are the same for each half of the low frequency cycle, conduction losses will be calculated for a primary current half-period.

$$P_{QP(con)} = \frac{1}{\pi}\int_{\phi}^{\phi+\pi}\left[V_{QPO}\hat{I}_P \sin(\theta-\phi) + r_{QP}\hat{I}_P{}^2 \sin^2(\theta-\phi)\right] m_a \sin\theta d\theta$$

$$= \frac{1}{2}V_{QPO}\hat{I}_P m_a \cos\phi + \frac{4m_a r_{QP}\hat{I}_P{}^2}{3\pi}\cos\phi \tag{7-10a}$$

The secondary switches conduct on alternate half-cycles. Hence, the total loss is given by the following equation in which the integration limits are set to simplify the solution, which is independent of phase.

$$P_{QS(con)} = \frac{1}{\pi}\int_0^{\pi}\left(V_{QSO} i_S + r_{QS} {i_S}^2\right)d\theta = \frac{V_{QSO}}{\pi}\int_0^{\pi}\frac{\hat{I}_P}{N}\sin\theta d\theta + \frac{r_{QS}}{\pi}\int_0^{\pi}\left(\frac{\hat{I}_P}{N}\sin\theta\right)^2 d\theta$$

$$= \frac{2V_{QSO}\hat{I}_P}{\pi N} + \frac{r_{QS}{\hat{I}_P}^2}{2N^2} \qquad \text{(7-10b)}$$

Adding Eq's (7-10a) and (7-10b) gives the total switch conduction losses as:

$$P_{Q(con)} = \frac{1}{2}V_{QPO}\hat{I}_P m_a \cos\phi + \frac{4m_a r_{QP}{\hat{I}_P}^2}{3\pi}\cos\phi + \frac{2V_{QSO}\hat{I}_P}{\pi N} + \frac{r_{QS}{\hat{I}_P}^2}{2N^2} \qquad \text{(7-10c)}$$

7-1-4-2 Diode conduction loss

D_1 and D_2 conduct the same current waveforms on alternate half-cycles. Hence, the total conduction loss is given by:

$$P_{D(con)} = \frac{1}{\pi}\sum_{\phi}^{\phi+\pi}\left(V_{DO} i + r_D i^2\right)\Delta\theta_D$$

$$= \frac{1}{\pi}\int_{\phi}^{\phi+\pi}\left\{V_{DO}\frac{\hat{I}_P}{N}\sin(\theta-\phi) + r_D\left[\frac{\hat{I}_P}{N}\sin(\theta-\phi)\right]^2\right\}\left(m_a\sin\theta + 1 - m_a\sin\theta\right)d\theta$$

$$= \frac{2V_{DO}\hat{I}_P}{\pi N} + \frac{r_D{\hat{I}_P}^2}{2N^2} \qquad \text{(7-10d)}$$

7-1-5 High-frequency double-ended forward-converter inverters

Eq's (7-10c) and (7-10d) are also applied to double-ended forward-converter inverters except that primary-switch loss is multiplied by 2, as follows, because an additional switch is required.

$$P_{Q(con)} = V_{QPO}\hat{I}_P m_a \cos\phi + \frac{8m_a r_{QP}\hat{I}_P{}^2}{3\pi}\cos\phi + \frac{2V_{QSO}\hat{I}_P}{\pi N} + \frac{r_{QS}\hat{I}_P{}^2}{2N^2} \quad (7\text{-}11a)$$

$$P_{D(con)} = \frac{2V_{DO}\hat{I}_P}{\pi N} + \frac{r_D\hat{I}_P{}^2}{2N^2} \quad (7\text{-}11b)$$

7-1-6 High-frequency push-pull inverters

7-1-6-1 Switch conduction loss

For one primary switch:

$$P_{Qp(con)} = \frac{1}{4}V_{QPO}\hat{I}_P m_a \cos\phi + \frac{2m_a r_{QP}\hat{I}_P{}^2}{3\pi}\cos\phi \quad (7\text{-}12a)$$

The total switch conduction losses including secondary switches are:

$$P_{Q(con)} = \frac{1}{2}V_{QPO}\hat{I}_P m_a \cos\phi + \frac{4m_a r_{QP}\hat{I}_P{}^2}{3\pi}\cos\phi + \frac{2V_{QSO}\hat{I}_P}{\pi N} + \frac{r_{QS}\hat{I}_P{}^2}{2N^2} \quad (7\text{-}12b)$$

7-1-6-2 Diode conduction loss

Total diode conduction loss is given by:

$$P_{D(con)} = \frac{1}{\pi}\left\{\sum_{\phi}^{\phi+\pi}\left(V_{DO}i_D + r_D i_D{}^2\right)m_a \sin\theta\Delta\theta + 2\sum_{\phi}^{\phi+\pi}\left[V_{DO}\frac{i_D}{2} + r_D\left(\frac{i_D}{2}\right)^2\right](1 - m_a\sin\theta)\Delta\theta\right\}$$

$$\approx \frac{1}{\pi}\int_{\phi}^{\phi+\pi}\left\{V_{DO}\frac{\hat{I}_P}{N}\sin(\theta-\phi) + r_D\left[\frac{\hat{I}_P}{N}\sin(\theta-\phi)\right]^2\right\}m_a\sin\theta d\theta + \frac{1}{\pi}\int_{\phi}^{\phi+\pi}\left\{V_{DO}\frac{\hat{I}_P}{N}\sin(\theta-\phi) + r_D\frac{\left[\hat{I}_P\sin(\theta-\phi)\right]^2}{2N^2}\right\}(1 - m_a\sin\theta)d\theta$$

$$= \frac{1}{\pi}\left\{\int_{\phi}^{\phi+\pi} V_{DO}\frac{\hat{I}_P}{N}\sin(\theta-\phi)d\theta + \int_{\phi}^{\phi+\pi}\frac{r_D\hat{I}_P{}^2 m_a}{2N^2}\sin^2(\theta-\phi)\sin\theta d\theta + \right.$$

$$\left.\int_{\phi}^{\phi+\pi}\frac{r_D\hat{I}_P{}^2}{2N^2}\sin^2(\theta-\phi)d\theta\right\}$$

$$= \frac{2V_{DO}\hat{I}_P}{\pi N} + \frac{2r_D m_a\hat{I}_P{}^2}{3N^2\pi}\cos\phi + \frac{r_D\hat{I}_P{}^2}{4N^2} \qquad (7\text{-}12c)$$

7-1-7 High-frequency half-bridge inverters

$$P_{Q(con)} = \frac{1}{2}V_{QPO}\hat{I}_P m_a\cos\phi + \frac{4m_a r_{QP}\hat{I}_P{}^2}{3\pi}\cos\phi + \frac{2V_{QSO}\hat{I}_P}{\pi N} + \frac{r_{QS}\hat{I}_P{}^2}{2N^2} \qquad (7\text{-}13a)$$

$$P_{D(con)} = \frac{2V_{DO}\hat{I}_P}{\pi N} + \frac{2r_D m_a\hat{I}_P{}^2}{3N^2\pi}\cos\phi + \frac{r_D\hat{I}_P{}^2}{4N^2} \qquad (7\text{-}13b)$$

7-1-8 High-frequency full-bridge inverters

Total switch and diode conduction losses are given by Eq's (7-14a) and (7-14b).

$$P_{Q(con)} = V_{QPO}\hat{I}_P m_a\cos\phi + \frac{8m_a r_{QP}\hat{I}_P{}^2}{3\pi}\cos\phi + \frac{2V_{QSO}\hat{I}_P}{\pi N} + \frac{r_{QS}\hat{I}_P{}^2}{2N^2} \qquad (7\text{-}14a)$$

$$P_{D(con)} = \frac{2V_{DO}\hat{I}_P}{\pi N} + \frac{2r_D m_a\hat{I}_P{}^2}{3N^2\pi}\cos\phi + \frac{r_D\hat{I}_P{}^2}{4N^2} \qquad (7\text{-}14b)$$

7-1-9 Low-frequency half-bridge inverters without transformer

The switch and diode conduction losses of low-frequency half-bridge inverters without a transformer are approximately the same as those with a transformer and are given by Eq's (7-15a) and (7-15b).

$$P_{Q(con)} \approx \hat{I}_P V_{QO}\left(\frac{1}{\pi} + \frac{m_a}{4}\cos\phi\right) + 2r_Q\hat{I}_P{}^2\left(\frac{1}{8} + \frac{m_a}{3\pi}\cos\phi\right) \qquad (7\text{-}15a)$$

$$P_{D(con)} = \hat{I}_P V_{DO}\left(\frac{1}{\pi} - \frac{m_a}{4}\cos\phi\right) + 2r_D\hat{I}_P{}^2\left(\frac{1}{8} - \frac{m_a}{3\pi}\cos\phi\right) \quad (7\text{-}15b)$$

7-1-10 Low-frequency full-bridge inverters without transformer

The conduction losses of low-frequency full-bridge inverters without a transformer are the same as those with a transformer and are given by Eq's (7-16a) and (7-16b).

$$P_{D(con)} = 2\hat{I}_P V_{QO}\left(\frac{1}{\pi} + \frac{m_a}{4}\cos\phi\right) + 4r_Q\hat{I}_P{}^2\left(\frac{1}{8} + \frac{m_a}{3\pi}\cos\phi\right) \quad (7\text{-}16a)$$

$$P_{D(con)} = 2\hat{I}_P V_{DO}\left(\frac{1}{\pi} - \frac{m_a}{4}\cos\phi\right) + 4r_D\hat{I}_P{}^2\left(\frac{1}{8} - \frac{m_a}{3\pi}\cos\phi\right) \quad (7\text{-}16b)$$

Table (7-1) summarises the conduction losses for different dc/ac inverter topologies. It can be seen that conduction losses are proportional to the primary-current peak, $\hat{I}_P$, and the switch on-state resistance, r_Q. Wherever possible, these parameter values should be reduced in order to reduce conduction power-loss.

It is difficult using the equations in Table (7-1) to make direct comparisons of total conduction-loss between the topologies because it is not possible to normalise the equations further. Also, device conduction properties, i.e. r_Q, r_D, V_{QO}, V_{DO} and transformer ratio, N, vary between some topologies. It is therefore necessary to design inverters to operate under specific conditions, and thereby calculate numeric power-loss values for each topology, which can then be easily compared, as is done in the following sections.

However, an equivalent table of switching power-loss equations must first be derived which may be added to give total inverter power-loss and hence efficiency.

No.	Topology	Conduction losses
1	L.F. Push-pull	$V_{QO}\hat{I}_P\left(\frac{1}{\pi}+\frac{m_a}{4}\cos\phi\right)+2r_Q\hat{I}_P{}^2\left(\frac{1}{8}+\frac{m_a}{3\pi}\cos\phi\right)+V_{DO}\hat{I}_P\left(\frac{1}{\pi}-\frac{m_a}{4}\cos\phi\right)+2r_D\hat{I}_P{}^2\left(\frac{1}{8}-\frac{m_a}{3\pi}\cos\phi\right)$
2	L.F. Half-Bridge	$V_{QO}\hat{I}_P\left(\frac{1}{\pi}+\frac{m_a}{4}\cos\phi\right)+2r_Q\hat{I}_P{}^2\left(\frac{1}{8}+\frac{m_a}{3\pi}\cos\phi\right)+V_{DO}\hat{I}_P\left(\frac{1}{\pi}-\frac{m_a}{4}\cos\phi\right)+2r_D\hat{I}_P{}^2\left(\frac{1}{8}-\frac{m_a}{3\pi}\cos\phi\right)$
3	L.F. Full-Bridge	$2V_{QO}\hat{I}_P\left(\frac{1}{\pi}+\frac{m_a}{4}\cos\phi\right)+4r_Q\hat{I}_P{}^2\left(\frac{1}{8}+\frac{m_a}{3\pi}\cos\phi\right)+2V_{DO}\hat{I}_P\left(\frac{1}{\pi}-\frac{m_a}{4}\cos\phi\right)+4r_D\hat{I}_P{}^2\left(\frac{1}{8}-\frac{m_a}{3\pi}\cos\phi\right)$
4	H.F. S-E Forward	$\frac{1}{2}V_{QPO}\hat{I}_P m_a\cos\phi+\frac{4m_a r_{QP}\hat{I}_P{}^2}{3\pi}\cos\phi+\frac{2V_{QSO}\hat{I}_P}{\pi N}+\frac{r_{QS}\hat{I}_P{}^2}{2N^2}+\frac{2V_{DO}\hat{I}_P}{N\pi}+\frac{r_D\hat{I}_P{}^2}{2N^2}$
5	H.F. D-E Forward	$V_{QPO}\hat{I}_P m_a\cos\phi+\frac{8m_a r_{QP}\hat{I}_P{}^2}{3\pi}\cos\phi+\frac{2V_{QSO}\hat{I}_P}{\pi N}+\frac{r_{QS}\hat{I}_P{}^2}{2N^2}+\frac{2V_{DO}\hat{I}_P}{N\pi}+\frac{r_D\hat{I}_P{}^2}{2N^2}$
6	H.F. Push-Pull	$\frac{1}{2}V_{QPO}\hat{I}_P m_a\cos\phi+\frac{4m_a r_{QP}\hat{I}_P{}^2}{3\pi}\cos\phi+\frac{2V_{QSO}\hat{I}_P}{\pi N}+\frac{r_{QS}\hat{I}_P{}^2}{2N^2}+\frac{2V_{DO}\hat{I}_P}{\pi N}+\frac{2r_D m_a\hat{I}_P{}^2}{3\pi N^2}\cos\phi+\frac{r_D\hat{I}_P{}^2}{2N^2}$
7	H.F. Half-Bridge	$\frac{1}{2}V_{QPO}\hat{I}_P m_a\cos\phi+\frac{4m_a r_{QP}\hat{I}_P{}^2}{3\pi}\cos\phi+\frac{2V_{QSO}\hat{I}_P}{\pi N}+\frac{r_{QS}\hat{I}_P{}^2}{2N^2}+\frac{2V_{DO}\hat{I}_P}{\pi N}+\frac{2r_D m_a\hat{I}_P{}^2}{3\pi N^2}\cos\phi+\frac{r_D\hat{I}_P{}^2}{2N^2}$
8	H.F. Full-Bridge	$V_{QPO}\hat{I}_P m_a\cos\phi+\frac{8m_a r_{QP}\hat{I}_P{}^2}{3\pi}\cos\phi+\frac{2V_{QSO}\hat{I}_P}{\pi N}+\frac{r_{QS}\hat{I}_P{}^2}{2N^2}+\frac{2V_{DO}\hat{I}_P}{\pi N}+\frac{2r_D m_a\hat{I}_P{}^2}{3\pi N^2}\cos\phi+\frac{r_D\hat{I}_P{}^2}{2N^2}$

Table 7-1 Conduction power losses for dc/ac inverter topologies

7-2 SWITCHING POWER LOSS CALCULATIONS

Switching losses comprise turn-on and turn-off losses for both power switches, rectifiers and freewheeling diodes. Diode turn-on losses due to forward recovery will be ignored because this is generally low in comparison with the switching loss associated with the reverse-recovery effect. During the reverse-recovery effect at turn-off, the voltage across the diode does not reverse until most of the stored charge, Q_{RR}, has been removed or recombined. At the end of reverse-recovery, when the reverse diode current drops to zero, turn-off losses in the diode have also been shown to be relatively small and may be neglected [1].

The main effect of the diode reverse-recovery current transient is to significantly increase switch turn-on switching loss and this will be considered in the next section.

Switching losses for the secondary-side switches have little effect on the total losses, as these switches are working at low frequencies. Therefore, switching losses for these devices have been neglected.

7-2-1 Turn-off switching losses

The turn-off energy loss may be given by Eq. (7-17) if the voltage rise time, T_{VR}, and the current fall time, T_{CF}, are theoretically calculated as shown in Fig. 7-1. App. (7-1) gives more details on rise- and fall-times measurements.

$$W_{Q(off)} = \frac{1}{2} VI(\theta)(T_{VR} + T_{CF}) \tag{7-17}$$

In Eq. (7-17), V is the switch drain-source voltage when it is turned off. This voltage varies for each topology. In single-ended forward and push-pull circuits, it is $2V_{DC}$, and it is V_{DC} in all other circuits.

In PWM inverters, the d.c. voltage is assumed constant, and hence T_{VR} will also be assumed constant. The turned-off current varies sinusoidally; hence T_{CF} will be assumed to vary sinusoidally and according to Eq. (7-18).

$$T_{CF}(\theta) = \hat{T}_{CF} \sin\theta = \frac{\hat{I}_P}{di/dt} \sin\theta \qquad (7\text{-}18)$$

where $\hat{T}_{CF}$ is the maximum current fall time taken at the primary peak current.

To obtain the turn-off power from the turn-off energy, Eq. (7-17) should be divided by the switching period T_S or $1/f_{SW}$. The total average power may then be estimated by averaging the total energy over a complete low-frequency switching-cycle period. If the switching period is assumed to be reduced to a very small value, then the discrete switching power-loss equations may be approximated by the continuous system integrals for the various inverter types, as follows.

7-2-1-1 Low-frequency push-pull inverters

In this topology, devices must switch $2V_{DC}$, $I(\theta)$ is $\hat{I}_P \sin\theta$, and turn-off switching waveform crossover time is $(T_{VR} + \hat{T}_{CF} \sin\theta)$. Total average turn-off switching power-loss for the two switches is, therefore:

$$P_{Q(off)} = \frac{1}{\pi}\int_0^{\pi} \frac{1}{2} f_{SW}(2V_{DC})\hat{I}_P \sin\theta\left(T_{VR} + \hat{T}_{CF}\sin\theta\right)d\theta$$

$$= \frac{1}{\pi} f_{SW} V_{DC} \hat{I}_P \left(T_{VR}\int_0^{\pi} \sin\theta d\theta + \hat{T}_{CF}\int_0^{\pi} \sin^2\theta d\theta \right)$$

$$= \frac{1}{\pi} f_{SW} V_{DC} \hat{I}_P \left[2T_{VR} + \hat{T}_{CF}\left(\frac{1}{2}\theta - \frac{1}{4}\sin 2\theta\right)_0^{\pi} \right]$$

$$= \frac{1}{\pi} f_{SW} V_{DC} \hat{I}_P \left(2T_{VR} + \frac{\pi}{2}\hat{T}_{CF} \right)$$

$$P_{Q(off)} = \frac{1}{2\pi} f_{SW} V_{DC} \hat{I}_P \left(4T_{VR} + \pi\hat{T}_{CF}\right) \qquad (7\text{-}19)$$

7-2-1-2 Turn-off switching losses in other inverter topologies

Eq. (7-19) may also be applied to topologies 3, 4, 5, and 8, as listed in Table (7-2), whereas in topologies 2, 6, and 7, the turn-off switching power loss is half that given by Eq. (7-19).

7-2-2 Turn-on switching losses

Switch turn-on loss is significantly affected by freewheel-diode reverse recovery effect. This is normally specified as a reverse-recovery charge, Q_{RR}, in diode data sheets and this must therefore be used to calculate turn-on switching loss.
As described in [1], Eq. (7-20) may be used to estimate the turn-on switching losses in one leg of a bridge inverter. The same may be applied to topologies 2, 4, 6, and 7, whereas in topologies 1, 3, 5, and 8, this should be multiplied by 2.

$$P_{Q(on)} = \frac{f_{SW} V_{DC}}{2\pi}\left(2\frac{\hat{I}_P}{I_{DR}} Q_{RRR} + 2.472\hat{I}_P\sqrt{\frac{Q_{RRR}\hat{I}_P / I_{DR}}{di/dt}} + \frac{\pi \hat{I}_P{}^2}{4di/dt}\right) \tag{7-20}$$

where Q_{RRR} is the reverse recovery charge at a specified current, I_{DR}, which may be taken from the data sheet, and *di/dt* is the rate of change of the current anticipated in the application.

7-2-3 Switch output capacitance switching losses

Additional switch turn-on loss produced by the device output capacitance, C_{OSS}, should also be included in the total losses as shown in Eq. (7-21) for each power switch.

$$P_{COSS} = f_{SW}\left(\frac{1}{2} C_{OSS} V^2\right) \tag{7-21}$$

where V is the switch drain-source, or collector-emitter, voltage when the switch is turned-off. This voltage differs from one topology to another and equals $V_{DC(min)}$ in half-bridge, full-bridge and double-ended forward-converter inverters, and equals $2V_{DC(min)}$ in push-pull and single-ended forward-converter inverters neglecting the leakage inductance spikes.

Table (7-2) summarises the switching losses for different dc/ac inverter topologies. In this table, it can be seen that the switching loss is directly proportional to the switching frequency, f_{SW}. Once again, loss equations cannot be normalised for easy direct comparison. Hence, both sets of conduction [Table (7-1)] and switching [Table (7-2)] loss equations will now be used to calculate the total loss in specific designs.

7-3 DESIGN EXAMPLE

An inverter example with the following specifications is used to illustrate how the power loss and efficiency of all the above inverters vary with frequency:

Output power, $P_O = 200W$

Input voltage, $V_{IN} = 120Vrms$, which gives

$V_{DC(min)} = 125V$ and

$V_{DC(max)} = 190V$.

The following power MOSFET's were selected for each of the inverter types:

IRF830 for the push-pull inverter,

IRF630 for the double-ended forward, half- and full-bridge inverters, and

IRF840 for the single-ended forward-converter inverter.

Fast recovery diode type MUR450 was selected for all inverter topologies.

Fig's 7-2a to h show turn-on, P_{ON}, turn-off, P_{OFF} and switch output capacitance, P_C, switching losses, switch and diode conduction losses, P_Q and P_D, and finally the total power losses for each inverter topology and for the above example. Parameter values used to estimate switching and conduction power-loss are given in App. (7-2) for each topology [2, 3].

No.	Topology	Switching losses
1	L.F. Push-pull	$\frac{1}{2\pi} f_{SW} V_{DC} \hat{I}_P \left(4T_{VR} + \pi \frac{\hat{I}_P}{di/dt} \right) + \frac{f_{SW} V_{DC}}{\pi} \left(2 \frac{\hat{I}_P}{I_{DR}} Q_{RRR} + 2.472 \hat{I}_P \sqrt{\frac{Q_{RRR} \hat{I}_P / I_{DR}}{di/dt} + \frac{\pi \hat{I}_P^2}{4di/dt}} \right) + 4 f_{SW} C_{OSS} V_{DC}^2$
2	L.F. Half-Bridge	$\frac{1}{4\pi} f_{SW} V_{DC} \hat{I}_P \left(4T_{VR} + \pi \frac{\hat{I}_P}{di/dt} \right) + \frac{f_{SW} V_{DC}}{2\pi} \left(2 \frac{\hat{I}_P}{I_{DR}} Q_{RRR} + 2.472 \hat{I}_P \sqrt{\frac{Q_{RRR} \hat{I}_P / I_{DR}}{di/dt} + \frac{\pi \hat{I}_P^2}{4di/dt}} \right) + f_{SW} C_{OSS} V_{DC}^2$
3	L.F. Full-Bridge	$\frac{1}{2\pi} f_{SW} V_{DC} \hat{I}_P \left(4T_{VR} + \pi \frac{\hat{I}_P}{di/dt} \right) + \frac{f_{SW} V_{DC}}{\pi} \left(2 \frac{\hat{I}_P}{I_{DR}} Q_{RRR} + 2.472 \hat{I}_P \sqrt{\frac{Q_{RRR} \hat{I}_P / I_{DR}}{di/dt} + \frac{\pi \hat{I}_P^2}{4di/dt}} \right) + 2 f_{SW} C_{OSS} V_{DC}^2$
4	H.F. S-E Forward	$\frac{1}{2\pi} f_{SW} V_{DC} \hat{I}_P \left(4T_{VR} + \pi \frac{\hat{I}_P}{di/dt} \right) + \frac{f_{SW} V_{DC}}{2\pi} \left(2 \frac{\hat{I}_P}{I_{DR}} Q_{RRR} + 2.472 \hat{I}_P \sqrt{\frac{Q_{RRR} \hat{I}_P / I_{DR}}{di/dt} + \frac{\pi \hat{I}_P^2}{4di/dt}} \right) + 2 f_{SW} C_{OSS} V_{DC}^2$
5	H.F. D-E Forward	$\frac{1}{2\pi} f_{SW} V_{DC} \hat{I}_P \left(2T_{VR} + \pi \frac{\hat{I}_P}{di/dt} \right) + \frac{f_{SW} V_{DC}}{\pi} \left(2 \frac{\hat{I}_P}{I_{DR}} Q_{RRR} + 2.472 \hat{I}_P \sqrt{\frac{Q_{RRR} \hat{I}_P / I_{DR}}{di/dt} + \frac{\pi \hat{I}_P^2}{4di/dt}} \right) + f_{SW} C_{OSS} V_{DC}^2$
6	H.F. Push-Pull	$\frac{1}{4\pi} f_{SW} V_{DC} \hat{I}_P \left(4T_{VR} + \pi \frac{\hat{I}_P}{di/dt} \right) + \frac{f_{SW} V_{DC}}{2\pi} \left(2 \frac{\hat{I}_P}{I_{DR}} Q_{RRR} + 2.472 \hat{I}_P \sqrt{\frac{Q_{RRR} \hat{I}_P / I_{DR}}{di/dt} + \frac{\pi \hat{I}_P^2}{4di/dt}} \right) + 4 f_{SW} C_{OSS} V_{DC}^2$
7	H.F. Half-Bridge	$\frac{1}{4\pi} f_{SW} V_{DC} \hat{I}_P \left(4T_{VR} + \pi \frac{\hat{I}_P}{di/dt} \right) + \frac{f_{SW} V_{DC}}{2\pi} \left(2 \frac{\hat{I}_P}{I_{DR}} Q_{RRR} + 2.472 \hat{I}_P \sqrt{\frac{Q_{RRR} \hat{I}_P / I_{DR}}{di/dt} + \frac{\pi \hat{I}_P^2}{4di/dt}} \right) + f_{SW} C_{OSS} V_{DC}^2$
8	H.F. Full-Bridge	$\frac{1}{2\pi} f_{SW} V_{DC} \hat{I}_P \left(4T_{VR} + \pi \frac{\hat{I}_P}{di/dt} \right) + \frac{f_{SW} V_{DC}}{\pi} \left(2 \frac{\hat{I}_P}{I_{DR}} Q_{RRR} + 2.472 \hat{I}_P \sqrt{\frac{Q_{RRR} \hat{I}_P / I_{DR}}{di/dt} + \frac{\pi \hat{I}_P^2}{4di/dt}} \right) + 2 f_{SW} C_{OSS} V_{DC}^2$

Table 7-2 Switching losses for dc/ac inverter topologies

For example, Fig. 7-2a shows the power losses of the low-frequency push-pull inverter. From the figure, it can be seen that turn-on, turn-off and switch output capacitance switching power losses, P_{OFF}, P_{ON}, and P_C respectively, are directly proportional to switching frequency, f_{SW}, and give straight parallel line-graphs up to about 500kHz or so. At low f_{SW}, switching loss has little effect on the total inverter power loss. Above 500kHz or so, the value of switching loss quickly approaches and then exceeds the conduction power-loss.

Conduction losses, P_Q and P_D, are relatively independent of frequency, which are seen as horizontal lines up to about 200kHz. Above 200kHz, the total losses increase significantly as a result of rapidly increasing switching losses, and the efficiency is reduced. This increases the required primary current, as shown in Eq. (6-18), which further causes switching and conduction losses to increase more rapidly. This is seen in Fig. 7-2a as a slightly faster increase in all losses in the highest f_{SW} decade of the graph. The switching power loss associated with the switch output capacitance, is seen to have little effect on the total losses and, therefore, can be neglected at low voltage levels. The above pattern of loss variation applies with all inverter topologies, as shown in Fig's 7-2b to h.

To examine the effect of the d.c. supply voltage on power losses, the maximum d.c. supply voltage, $V_{DC(max)}$, was used to estimate the power losses in two inverters; high-frequency push-pull and full-bridge inverters. The result is shown in App. (7-3). It can be seen that conduction losses and, hence, total losses have been considerably reduced because the primary current is reduced (compare with Fig's 7-2f and h). However, the switch output capacitance switching loss approaches other switching-loss components more closely, because its value is proportional to supply-voltage-squared, and independent of the value of switched current. Turn-on and turn-off switching losses have decreased slightly because they are less dependent on the d.c. supply voltage than the primary current.

This condition of operating with the maximum utility a.c., and hence inverter d.c. supply voltage, resembles to some extent using a boost converter as a pre-regulator, which gives a high stable d.c. voltage for the inverter. This also has the advantage of considerably reducing the inverter operating current and, hence, total inverter power losses, since switching losses are approximately proportional to current and conduction losses are approximately proportional to current-squared.

Fig. 7-3a shows the total power losses, and Fig. 7-3b shows the efficiency for all inverter topologies thus described. However, these two figures must not be misinterpreted. The conduction power loss depends on the on-state resistance of the power MOSFET's, r_Q, and the dynamic resistance, r_D, of the power diodes as is shown earlier. MOSFET's having lower on-state resistance may be selected for inverters in which power switches block the d.c. supply voltage alone, such as half- and full-bridge circuits in both low- and high-frequency inverters and high-frequency double-ended forward-converter inverters. This considerably reduces power losses in these inverters because of the reduced on-resistance.

For example, the described single-ended forward-converter inverter uses IRF830 (500V/5.1A) power MOSFET which has 0.85Ω on-state resistance. The double-ended forward-converter inverter uses IRF630 (200V/5.7A) because of the reduced voltage stress in these inverters. The on-state resistance of this device is 0.4Ω. This, of course, reduces the MOSFET conduction power loss by a factor of 2, although for the same on-state resistance the double-ended forward-converter inverter dissipate higher power because of the added switch.

From Fig. 7-3 it can be seen that the low-frequency full-bridge inverter provides the maximum efficiency compared to all other inverters described so far. This is mainly due to being able to use MOSFET's with low on-state resistance as a result of the minimum voltage blocking requirements of V_{DC}.

The second choice is the high-frequency full-bridge inverter up to 200kHz. Beyond this frequency, The low-frequency push-pull circuit is the second choice. Forward-converter inverters have the minimum efficiency especially at high frequencies. This is mainly due to the high primary currents in these topologies.

From the above, it may be concluded that using high-frequency inverters, has the effect of reducing the weight and volume of the inverter transformer, but reduces the overall efficiency of the inverter especially at high frequency. The high-frequency full-bridge circuit may be implemented with very low on-state resistance MOSFET's to give lower volume high-frequency inverter systems than low-frequency equivalents with equivalent efficiency. However, the lower r_Q large-area MOSFET's will impose a cost penalty.

App. (7-4) lists a MATLAB program used to estimate and draw switching and conduction power losses for the high-frequency full-bridge inverter. All equations used in this program were taken from Ch's 6 and 7. The same program was used to compute the losses for the other topologies once the equations and parameters had been slightly modified to take into account differences in operating conditions.

CHAPTER SEVEN REFERENCES

1. F.V.P. Robinson, "Control of power semiconductor device switching", Ph.D thesis, December 1992, Chapter 3.
2. "Power MOSFET databook", International Rectifier, 1993.
3. "MOTOROLA Rectifier Device Data", DL 151/D, 1992.

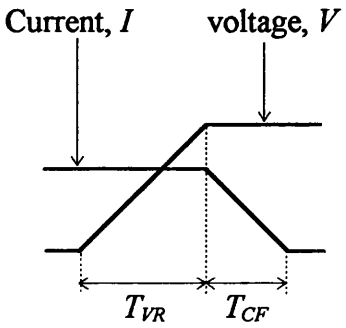
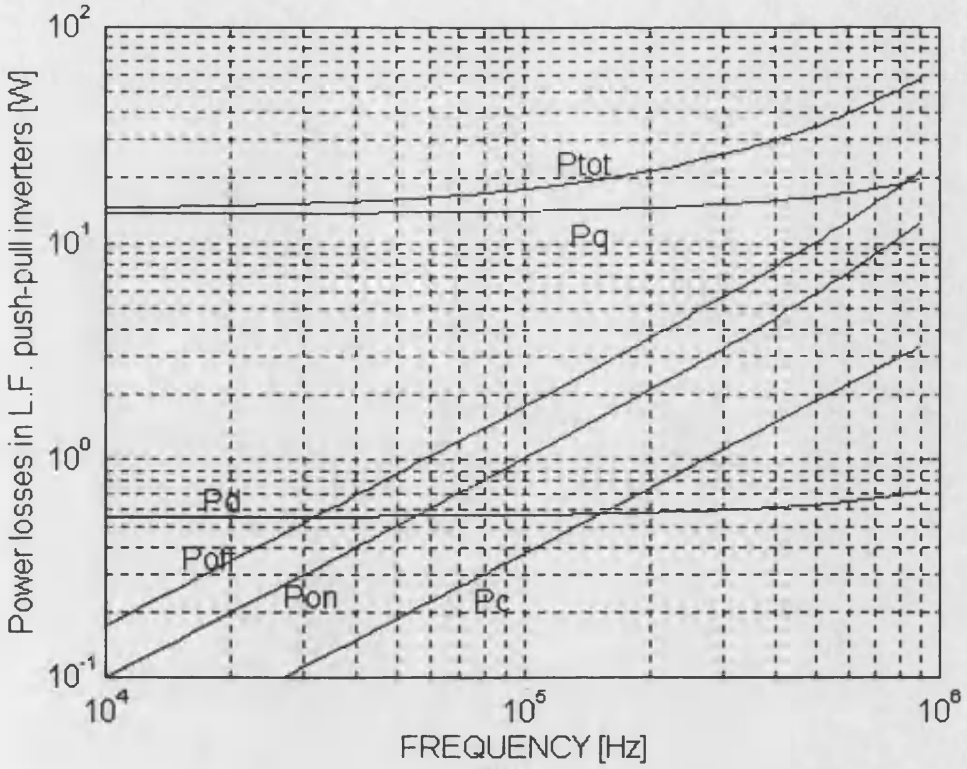
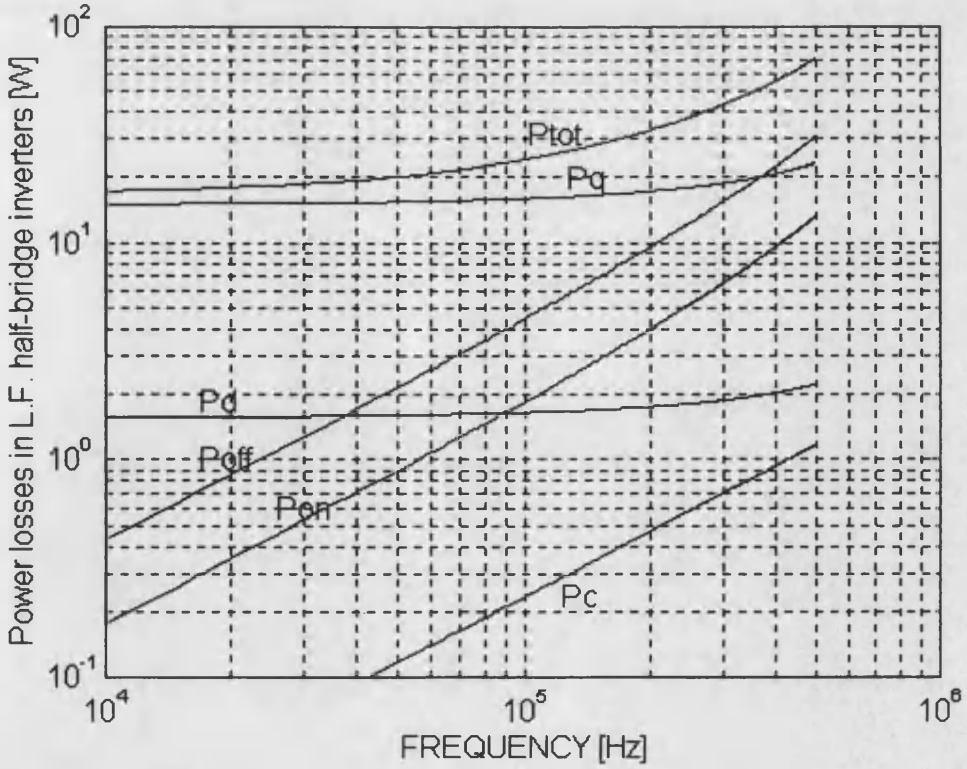


Fig. 7-1 The definition of voltage-rise and current-fall times [see App. (7-1)]

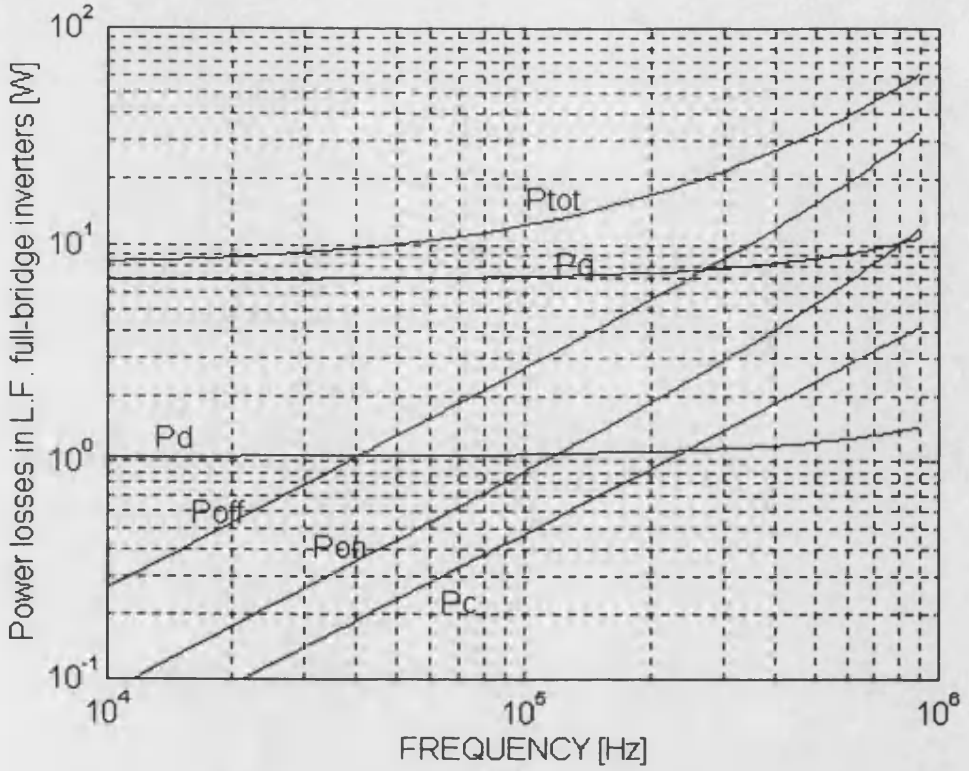


(a)



(b)

Fig. 7-2 Power losses versus f_{SW} in a) low-frequency push-pull and b) low-frequency half-bridge inverters



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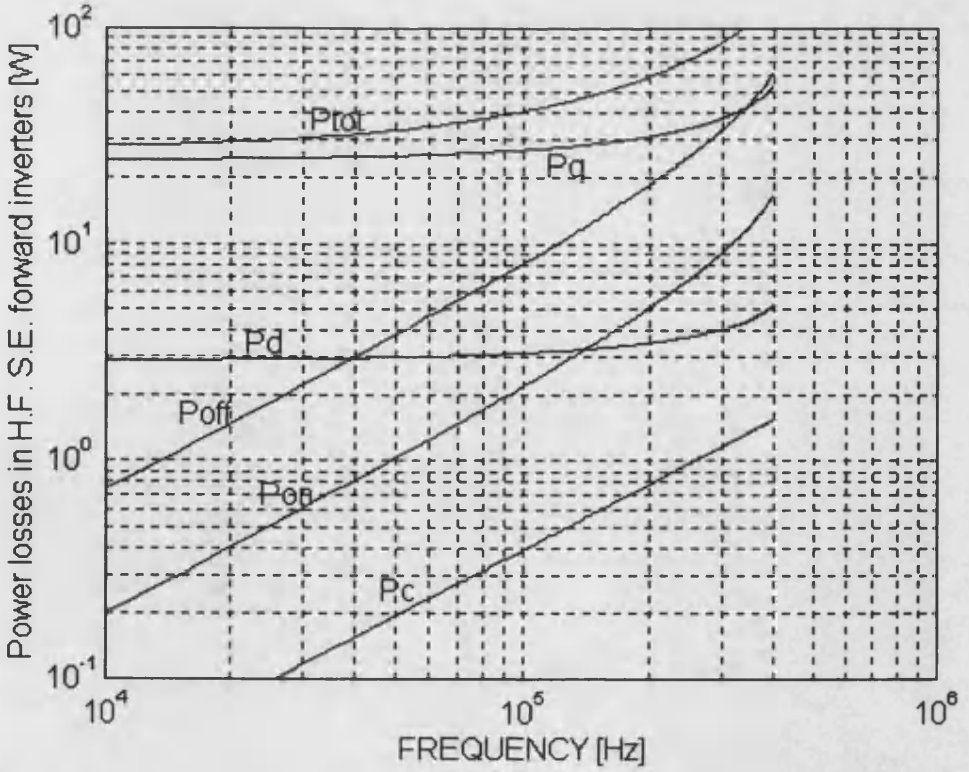
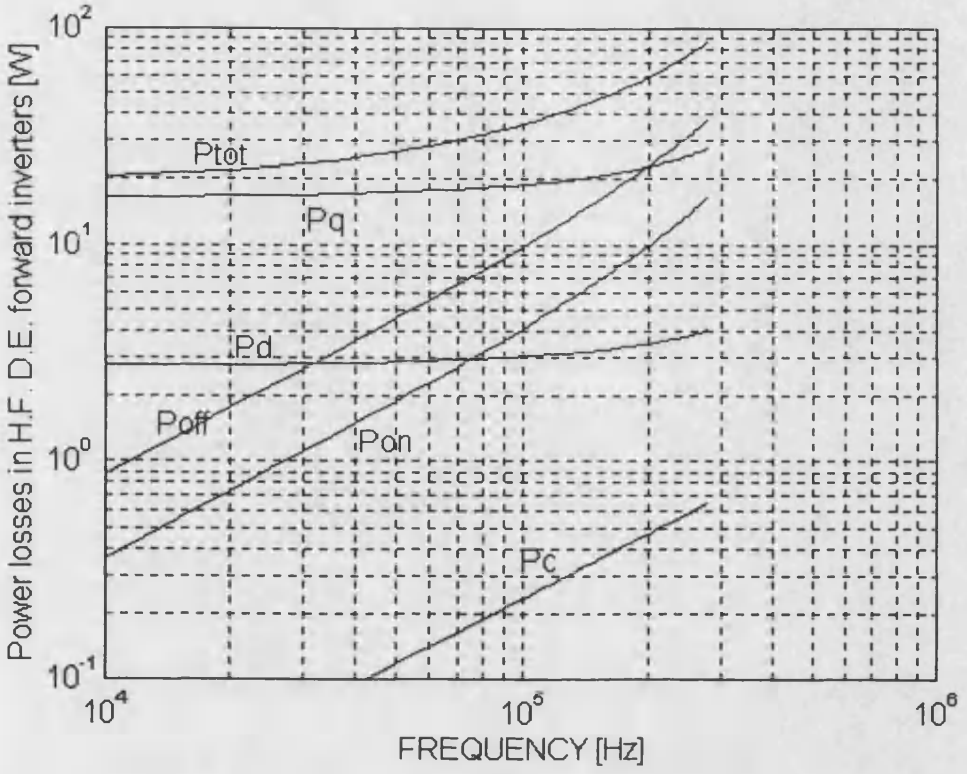
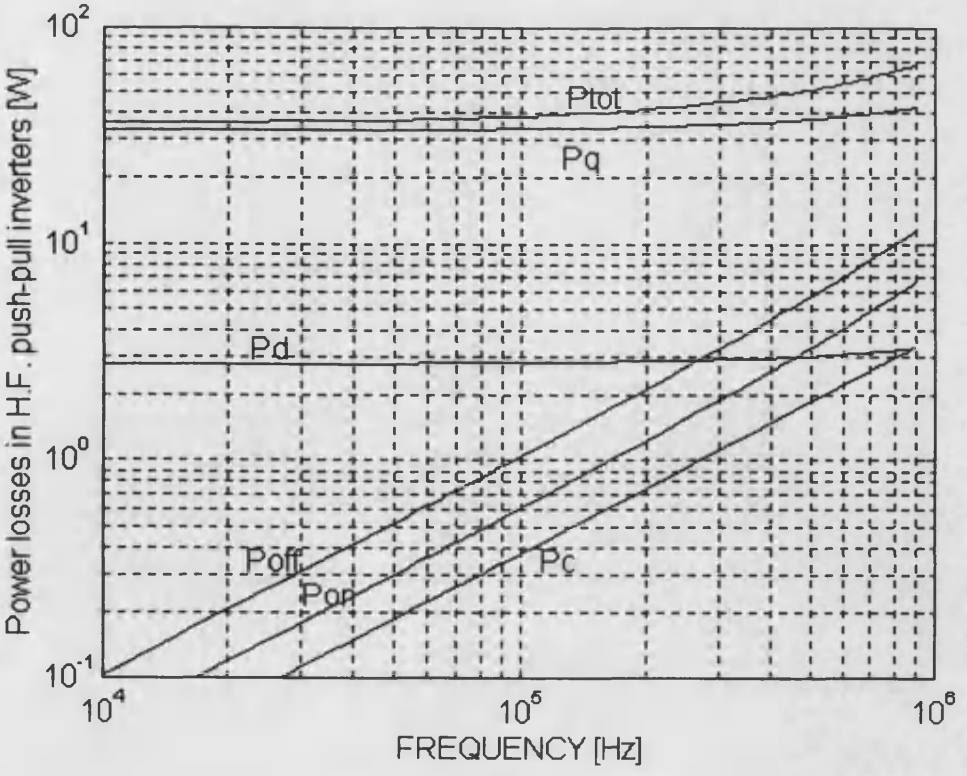


(d)

Fig. 7-2 Power losses versus f_{SW} in c) low-frequency full-bridge and d) high-frequency single-ended forward-converter inverters

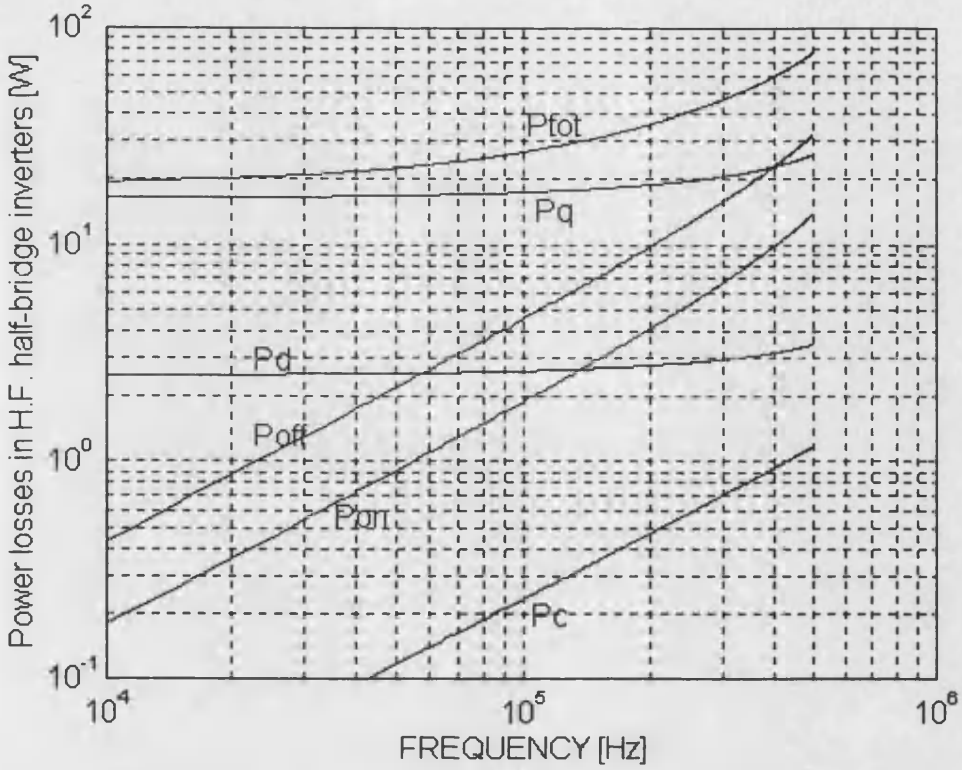


(e)

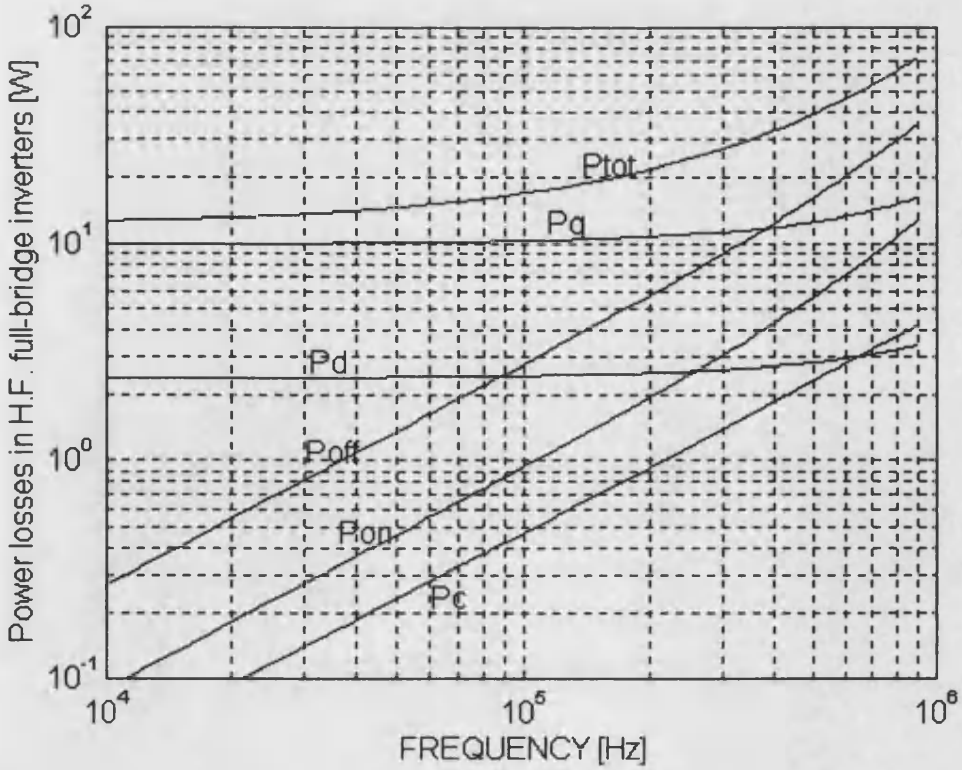


(f)

Fig. 7-2 Power losses versus f_{SW} in e) high-frequency double-ended forward-converter and f) high-frequency push-pull inverters

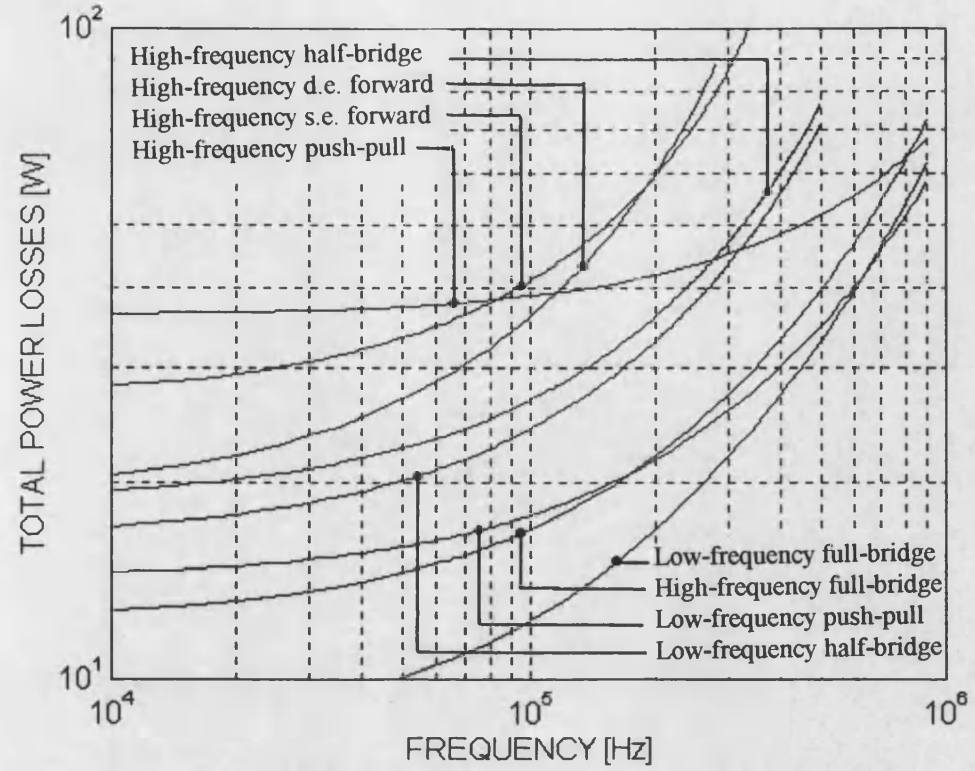


(g)

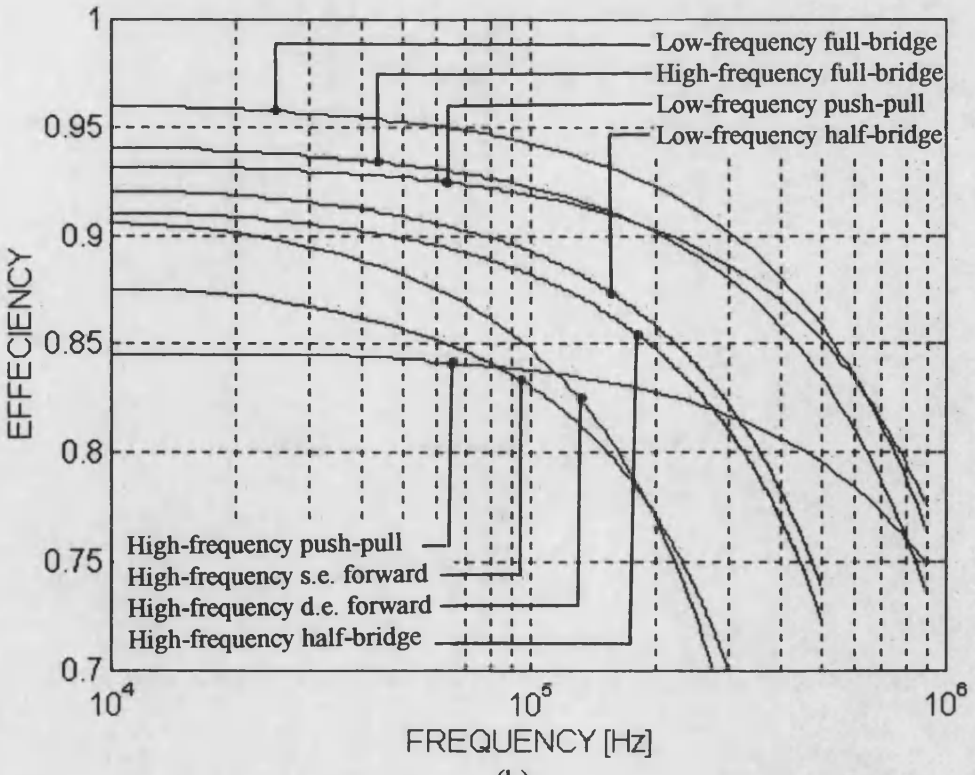


(h)

Fig. 7-2 Power losses versus f_{SW} in g) high-frequency half-bridge and h) high-frequency full-bridge inverters



(a)



(b)

Fig. 7-3 a) Total power losses and b) efficiency for dc/ac inverter topologies

LOW-FREQUENCY FULL-BRIDGE DC/AC INVERTER

8-1 INTRODUCTION

As described in Ch. 7, low-frequency full-bridge dc/ac inverters offer the highest efficiency due to their relatively small switch currents and voltage stress, especially if small on-state resistance power switches are employed. A low-frequency full-bridge inverter is, therefore, designed and thoroughly investigated.

Since the secondary and, therefore, the primary current can be in any direction irrespective of voltage polarity, freewheeling diodes should be used around the power switches. MOSFET's already have an integral diode between their drain and the source and form the simplest switch for this type of application. Another advantage of using MOSFET's is their simple drive and fast speed, which reduces power dissipation especially at high frequencies.

MOSFET's are, however, vulnerable to failure during inductive turn-off especially in full-bridge circuits. The main cause of the MOSFET failure in full-bridge dc/ac inverters is the high rate of change of the drain-source voltage, dV_{DS}/dt [1, 2], and the activation of the MOSFET parasitic bipolar transistor [1, 3]. This problem is discussed thoroughly in references [1, 2, 3] and solutions have been suggested.

It seems that, although the basic principles are very well-known, it is not an easy task to solve these problems in practice. Tens of transistors have been destroyed during the design and test of the full-bridge dc/ac inverter, which calls for a systematic study to be conducted to investigate the MOSFET failure and seek the possible remedies.

Practical considerations, where possible, have been discussed, and the effect of the layout on circuit performance has been highlighted and extensively supported by practical waveforms.

The effect of the value of the snubber resistor in full-bridge circuits on the power loss in the resistor, is mathematically analysed and simulated by PSPICE. Simulation results show a complete agreement with the mathematical analysis.

8-2 CIRCUIT DESCRIPTION

In order to investigate the problem of MOSFET's failure, the circuit shown in Fig. 8-2 was designed and practically tested. Attention has been paid to the layout of the power stage and the driving circuit which has a big influence on the MOSFET behaviour. Proper snubbers are connected right at the leads of the MOSFET's to eliminate any stray inductance due to leads length, which allowed the snubber capacitor values to be small, thus reducing the power loss associated with them.

At the beginning, and before involving the power transformer, a 33 Ω resistor in series with 10 mH inductor were used as a load. Also, lower voltage and current power MOSFET's were used (IRFI630G, 200V/5.4A), since they are much less expensive as those finally intended to be used (IRFP450, 500V/14A). Deliberate d.c. load current was introduced by making one part of the bridge (Q_2 and Q_4) conducts for longer time than the other part (Q_1 and Q_3). A pulse generator was used in this stage to generate the driving signals.

The sought specifications of the circuit are as follows:

Input voltage: 220 V a.c. /50 Hz

Output voltage: 220 V a.c. /400 Hz

Output power: 700 W

Switching frequency: 20 kHz

8-3 THE DEAD TIME

In full-bridge converters and inverters, before turning "on" one part of the bridge, say Q_1 and Q_3 in Fig. 8-2, the other part must be "off" some time ago to ensure that no short circuit across the d.c. rail occurs. This time is called the *dead time* where the four power switches are "off" at the same time, and no power is transferred from the input to the output.

The dead time depends primarily on the type of the switches used in the circuit, in addition to the expected voltages and currents. For bipolar devices, the dead time should be longer than the longest minority-carrier storage time of the switches under all operating conditions. For MOSFET's, since there is no minority-carrier storage effect, and only inter-terminal capacitance charging effect, the dead time can be very small. In theory, no dead time is required for MOSFET's, but practically pulses have rise and fall times due to parasitic elements in the circuit and MOSFET's internal capacitances. Therefore, it is recommended to have some dead time to ensure that no cross-conduction occurs. The dead time can be included using different methods as described in the next sections.

8-3-1 Inherent Dead Time in the Control Circuit

If a control circuit such as IR2110 series is used to control the power MOSFET's, an inherent dead exists between the output pulses [4], since the propagation delay of the turn-on pulse is 25 ns longer than that of the turn-off.

8-3-2 Resistor/Diode Pairs

If the internal dead time of the control circuit is not sufficient, or the employed control circuit has no dead time, a small resistor and a diode can be connected in parallel between the driver output and the gate of the MOSFET, as shown in Fig. 8-1a. When the "on" pulse is applied, i.e. when the output voltage of the driver is high, the input capacitance of the MOSFET, C_{GS}, charges through the small resistor

exponentially until V_{GS} reaches the threshold voltage of the MOSFET, at which time the MOSFET is turned "on" but delayed by a time depending on the driving pulse amplitude, the resistor value and C_{GS}. At turn-off, the input capacitance of the MOSFET, C_{iss} in this case, is discharged quickly through the diode and the output stage of the control circuit. Therefore, the turn-on is delayed while the turn-off is not, thus creating the required dead time. The diode should be fast, low signal diode, such as 1N4148, and needs not be a high voltage diode (few tens of volts would be enough). The resistor should be small non-inductive resistor, such as a 22 Ω carbon composition resistor.

This solution of introducing dead time is acceptable if the high *dV/dt* caused by the fast turn-off does not have any side effects, particularly at high d.c. voltages. If this is of a great problem (and it was in the designed circuit), another resistor can be connected in series with the diode, as shown in Fig. 8-1b, such that R_1 defines the speed of the turn-on and R_2 defines the speed of the turn-off. Of course, to ensure that the dead time still exists, R_1 must be larger than R_2. Alternatively, a small capacitor can be used as described in the following section.

8-3-3 Adding a Small Capacitor

As shown in Fig. 8-2, pull-up resistors are used at the output of the comparators, U_1 and U_2. If a small capacitor is connected between the output and ground (C_{16} and C_{17} in Fig. 8-2), then during the turn-on pulse, the capacitor delays the pulse for some time depending on the time constant $R_{16}C_{16}$ and $R_{17}C_{17}$, and the auxiliary supply voltage. During the turn-off, the capacitor discharges quickly in the output transistor of the comparator.

If it is required to reduce the turn-off speed of the MOSFET, a resistor should be connected at the output of the driver rather than at the output of the comparator, as described in the previous section.

In the designed circuit, it has been shown that using diode/resistor pairs to create the required dead time, was the main cause of the high dV_{DS}/dt which led to the MOSFET's failure. Therefore, only a small series resistor (22 Ω) is placed in the gate drive circuit to slow down the turn-off speed, while the dead time is created, as

described in the preceding section, at the output of the comparators and before the control IC.

8-4 PRACTICAL WAVEFORMS USING IRFI630G MOSFET'S

Fig's 8-3a, b, c and d show different voltage and current waveforms for the inverter shown in Fig. 8-2 at V_{DC} = 100 V, I_{LOAD} = 0.78 A, Q_1 and Q_3 on-time = 18.5 μs, Q_2 and Q_4 on-time = 30 μs, with a 2.2 nF and 18Ω/2W used as snubbers. Resistor/diode pairs are first used to create the required dead time which was about 0.4 μs. These waveform have been shown for comparison purposes when a different MOSFET type is used, as will be seen in the next section.

8-5 REPLACING POWER MOSFET'S

The power MOSFET's IRFI630G used in the previous circuit have been replaced by IRFP450 from IR. Fig. 8-4 shows V_{GS3} (upper trace) and V_{DS3} (middle trace). It seems that the voltage spike due to the primary leakage inductance is too high (about 100 V). To reduce this effect, two 100 nF/630V polyester decoupling capacitors are connected between the positive and negative d.c. supply voltage right at the switches terminals, and Fig. 8-4 (lower trace) was obtained. It seems that the added capacitors oscillate with stray circuit inductance at a frequency of about 860 kHz.
Most importantly is that the switches now work at much higher temperature. After about 10 min, the case temperature reached 70 °C and is still increasing. Also, the snubber resistors ran at much higher temperature (68 °C after 10 min), although exactly the same conditions are applied as in the previous circuit.

Fig's 8-5a, b and c show different waveforms at turn-on and turn-off, without the added two 100 nF capacitors. When the two capacitors are added, Fig. 8-6 is obtained which shows a high frequency oscillation but with a reduced voltage spike.

It is noticed from the turn-on and turn-off pulses that there is some overlap between the two pulses, which is certainly the reason behind the very high switches case and snubber resistors temperature. This overlap occurs since the internal capacitances of IRFP450 is much higher than those of IRFI630G (more than three times [5]).

To prove this, the dead time has to be increased from 0.4 μs to about 2.1 μs to ensure that the turn-off and turn-on pulses are completely separated. The technique used to add the required dead time is as described in Sec. (8-3-3) by connecting a 390 pF capacitor between the output of each comparator and ground. By doing so, the circuit has operated for more than an hour with the power switches and snubber resistors temperature not more than 33 °C. Fig's 8-7a, b and c show voltage and current waveforms after adding the 2.1 μs dead time. The figures show much better and well-understood behaviour of the transistor current. Clearly shown is the well-behaved reverse recovery current of the freewheeling diode (Fig. 8-7b, third trace). The negative-going current spike which was seen in Fig. 8-5c has been completely vanished.

In Fig's 8-7a, b and c, 10 Ω snubber resistors are used instead of 18 Ω to make snubber current measurements on the same scale as the power switch current to facilitate waveforms analysis.

To reduce the effect caused by the gate drive inductance, the output of the driver has to be rearranged to keep the gate drive inductance to a minimum. Therefore, the drive return for each MOSFET is kept very close to the control wire, the leads are very short and the gate resistance has very little inductance, which results in Fig's 8-8a, b, c and d. Comparing Fig. 8-8 with Fig. 8-7, sharp and much faster rise and fall times of the gate pulse can be clearly noticed. This of course has the effect of allowing for very short dead time to be used, since little overlap is expected between the turn-off pulse of one pair of the power switches and the turn-on pulse of the other pair. Fig. 8-8 also shows the dead time (upper trace) which is now about 2.1 μs.

The value of the two decoupling capacitors have been increased from 100 to 470 nF in order to reduce the effect of oscillation caused by adding them. Fig's 8-9a, b and c

show the result where better voltage and current waveforms even at high voltage and current values (280 V/5.5 A average current and 8 A peak current) are obtained.

8-6 CONNECTING POWER TRANSFORMER AND OUTPUT FILTER

After the improvement made to the drive circuit and the power stage of the inverter, the power transformer and output filter have been designed and connected in the circuit. The specifications of the transformer and the filter are given in the next two sections.

8-6-1 Transformer Design

The core used in this application is a C-core, type HWR70/24 with the following specifications [6]:

Lamination thickness: 0.3 mm,

Cross-sectional area : 5.75 cm^2,

Magnetic path length : 25.9 cm,

Power rating : 390 VA @ 50 Hz.

The assumed maximum flux density is 1 T, which leads to number of primary turns N_P = 300 turns. If it is assumed that the amplitude modulation m_a = 0.85, then the fundamental low frequency signal will also be 0.85 of the d.c. supply voltage. Therefore, the turns ratio must be:

$$N = \frac{N_S}{N_P} = \frac{1}{0.85} \approx 1.17$$

which gives N_S = 350 turns.

8-6-2 Filter Design

Since the required output frequency is 400 Hz, and the assumed switching frequency is 20 kHz, the required cut-off frequency of the output filter should lie in the range (1-10)kHz.

The available capacitor is 1.5 μF, and the inductance of the filter inductor is 1.86 mH @ 10 kHz. Therefore, the cut-off frequency is:

$$f_C = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{1.86\cdot 10^{-3}\cdot 1.5\cdot 10^{-6}}} \approx 3 \text{ kHz}$$

8-7 DISCUSSION AND PRACTICAL WAVEFORMS USING IRFP450 MOSFET'S

After connecting the complete inverter, the circuit was operating at full d.c. input voltage of 320 V and a power of 250 W. The amplitude modulation assumed is m_a = 0.85 which was used in the transformer design.

Fig. 8-10a shows the triangular high frequency waveform together with the sinewave low frequency waveform at the input of the comparators of Fig. 8-2. An expansion of this figure is given in Fig. 8-10b with one of the outputs of the comparators, where it is seen the pulse width modulated output. The other output is, of course, the reverse of this signal, and each output is applied at one part of the bridge. Fig. 8-10c shows the gate drive pulses and the drain-source voltage of one of the power MOSFET's.

Fig. 8-11 shows the output voltage of the transformer (the sinewave noisier trace) and the filter output (the sinewave signal which lies in the middle of the previous signal). The lower trace shows an expansion of the first trace where it is seen the high frequency oscillations due to the interwinding capacitance of the transformer.

This high frequency oscillation, in addition to increasing EMI, it increases the power loss in the transformer as the power loss is proportional to the square of the frequency.

One method to cancel this high frequency oscillation is to reduce the interwinding capacitance of the transformer. Generally, this is not easy especially in high-power high-voltage transformers and if multiple layers are used as in the designed transformer.

Another technique to eliminate these high frequency signals is to reposition the output filter and place it at the primary rather than at the secondary side (Fig. 6-3c). Fig. 8-12 shows the power stage with the filter at the primary side, while Fig. 8-13 shows the input voltage to the filter (the pulse-width-modulated signal) and the output voltage which is the transformer primary voltage (the sinewave signal). It can be seen that the high frequency oscillation has been completely eliminated from the primary voltage, and, therefore, has no effect what so ever on the transformer.

The interference caused by the high rate of change of the voltage (1500V/μs) and current, produces a lot of noise on the low frequency signals. Fig. 8-14 (middle trace) shows the noise produced because of this interference on the sinewave low frequency signal at the input of the comparators. An expansion of one event has been captured (upper trace in Fig. 8-14), together with the gate-source voltage (lower trace). This shows that at switch turn-on, a high frequency of about 20 MHz and lasts for about 0.5 μs, is shown on the low frequency signal. If the comparators are fast enough to respond to this frequency, these high frequency oscillations can cause multiple switching for the power MOSFET's.

Also, what can help avoiding multiple switching of the power MOSFET's, is the pulse width discriminator in the MOSFET driver IR2110, which can block pulses that are shorter than 50 ns [4]. So the above high frequency oscillation did not affect the operation of the circuit and no multiple switching was occurred.

If other drivers are used, or if the oscillation frequency is smaller than the one shown in Fig. 8-14, then some methods to reduce this interference or cancel its effect should be used. One technique which may be used in such situations if other measures to eliminate this noise fail, is presented in the next section.

8-8 PREVENTING MULTIPLE SWITCHING

Multiple switching can occur due to noise in the control or modulated signal if the noise level is higher than the voltage which the comparator senses. Fig. 8-15 shows how noise can cause multiple switching to power switches. Fig. 8-16a shows a circuit used to prevent this effect, while Fig. 8-16b shows the resulting waveforms. The function of the circuit is as follows:

clk_1 and clk_2 are narrow pulses generated at each rising and falling edge of a square wave signal which is also used to produce the triangular high frequency signal. It is assumed that the low frequency signal has a lower amplitude than the high frequency signal such that if the driving pulse, say V_1 in Fig. 8-16b, starts before the peak of the triangular signal, it ends after this peak, and the clock signal, clk_1, occurs during this driving pulse. The same applies for the second driving pulse, V_2, and clk_2 occurs during this pulse. It is also assumed that the modulator waveforms, V_1 and V_2, contain sufficient noise to cause multiple switching, while the squarewave signal, V_S, is noise-free.

Usually, the noise has effect just after the turn-on of the power switch at the triangular wave and the sinewave crossings. Therefore, it is shown to have an effect at the beginning of the driving pulses, V_1 and V_2.

Let us start with clk_2 being high. This will resets A_2 and sets A_1, causing V_4 to be zero and enabling A_3. When clk_2 ends, the outputs of A_1 and A_2 stay as they are until clk_1 comes. When V_1 switches high, V_3 transfers to high as well as V_5 which is the final driving pulse. If V_1 falls due to noise, V_3 falls but this does not affect the state of A_5, and V_5 stays high. When V_1 goes high again, V_3 transfers to high and also this does not change the state of V_5. When clk_1 comes, A_1 is reset and A_2 is set, forcing V_3 to be zero and enabling A_4. This state stays until V_1 falls and V_2 rises, at which time V_4 rises causing V_5 to fall and V_6 to rise, thus generating an on-pulse to the second pair of the switches. Therefore, the output of A_5 will not see the noise in the PWM pulses and no multiple switching occurs.

8-9 THE EFFECT OF SNUBBER RESISTOR VALUES ON ENERGY LOSS IN THE SNUBBER RESISTORS

Fig. 8-17 shows a full-bridge inverter with *RC* snubber circuits and freewheeling diodes since the bridge is expected to work with load currents in any direction. It is assumed that the load current, I_O, is constant and flowing in the direction shown in Fig. 8-17.

It is assumed at the beginning that Q_2 and Q_4 are "on" and at the instant of turning "off", and Q_1 and Q_3 are "off". Also assumed is that the voltage drop across the power switches and the freewheeling diodes is zero when they are in a conduction state. Since all snubber capacitors and resistors have the same value, the symbol *C* and *R* are used to refer to the capacitor and resistor values.

8-9-1 Before Q_2 and Q_4 Turn-Off

When Q_2 and Q_4 are "on", the load current is flowing from V_{DC}, Q_4, the load, Q_2 and back to ground. The voltage at point *X* is V_{DC}, and the voltage at point *Y* is zero. Capacitors C_2 and C_4 are fully discharged, C_1 and C_3 are charged to V_{DC}, and no currents in the snubber circuits flow.

8-9-2 Time interval t_0-t_1

The energy stored in the inductive load is usually much greater than that stored in snubber capacitors. Hence, when Q_2 and Q_4 are turned "off", the right half of the bridge may be approximated to the circuit shown in Fig. 8-18a. The load current is still flowing in the load, but because Q_4 and D_3 are now "off", the load current flows in the snubber circuits as shown in the arrows in Fig. 8-18a. C_4 starts charging and C_3 discharging causing V_X to decrease. Because V_{DC} is constant and because of the symmetry, any change in V_X causes the same change in the voltage across C_3 and C_4, and, therefore, the same current flows in each snubber which is $I_O/2$, as shown in Fig. 8-19.

The change in voltage across C_3 will be:

$$V_{C3} = \frac{1}{C}\int_{t_0}^{t_1} i_S \, dt = \frac{1}{C}\int_{t_0}^{t_1} \frac{-I_O}{2} \, dt$$

$$V_{C3} = -\frac{I_O \Delta t}{2C} + V_{DC} \tag{8-1}$$

where $$\Delta t = t_1 - t_0 \tag{8-2}$$

Since I_O is approximately constant, the voltage across the capacitor decreases linearly with time (see Fig. 8-19).

As long as this voltage is higher than the voltage across R_3 (which is $RI_O/2$ during this period), V_X is still higher than zero, and D_3 is still in a non-conducting state. When these two voltages are equal, V_X will be zero and D_3 conducts at time $t = t_1$. Eq. (8-1) can now be written as:

$$\frac{I_O R}{2} = -\frac{I_O \Delta t}{2C} + V_{DC} \tag{8-3}$$

which gives a formula for Δt:

$$\Delta t = \frac{V_{DC} - RI_O/2}{I_O/(2C)} = \frac{2V_{DC} - RI_O}{I_O} C \tag{8-4}$$

During this period, the energy dissipated in R_3 is:

$$E_{R01} = R\int_{t_0}^{t_1} i_S^{\,2} \, dt = R\left(\frac{I_O}{2}\right)^2 \frac{2V_{DC} - RI_O}{I_O} C$$

$$E_{R01} = \frac{RI_O C}{2}\left(V_{DC} - \frac{RI_O}{2}\right) \tag{8-5}$$

8-9-3 Time Interval t_1-t_2

When D_3 conducts at time $t = t_1$, the circuit of Fig. 8-18a changes to the one in Fig. 8-18b. The voltage across C_3 is now given by:

$$V_{C3} = V_{C_{t=t1}} e^{-t/(RC)} = \frac{I_O R}{2} e^{-t/(RC)} \tag{8-6}$$

Therefore, the voltage reduces exponentially with a time constant RC.
The snubber current in R_3 will be:

$$i_s = \frac{I_o}{2} e^{-t/(RC)} \tag{8-7}$$

This interval (t_2-t_1) stays until all energy in C_3 has been dissipated. The energy dissipated in R_3 during this period can be given by:

$$E_{R12} = R\int i_s^2 \, dt = R\int (\frac{I_o}{2})^2 e^{-2t/(RC)} dt$$

$$E_{R12} = \frac{RI_o^2}{4}(-\frac{RC}{2} e^{-2t/(RC)})_{0\to\infty}$$

$$E_{R12} = \frac{RI_o^2}{4}\frac{RC}{2} = \frac{R^2 I_o^2 C}{8} \tag{8-8}$$

Eq. (8-8) can also be found as follows:
At time $t = t_1$, the voltage across C_3 is:

$$V_{C3} = \frac{RI_o}{2} \tag{8-9}$$

The energy stored in C_3 is now:

$$E_{C3} = \frac{1}{2} C V_{C3}^2 = \frac{1}{2} C (\frac{RI_o}{2})^2 = \frac{R^2 I_o^2 C}{8} \tag{8-10}$$

Since D_3 conducts the load current, all of this energy will be dissipated in R_3, as Eq. (8-8) shows.

In fact, the theoretical value of t_2 is infinity, but practically it can be assumed that the energy stored in the capacitor has been dissipated after about five time-constants, i.e. $5RC$, where the voltage and the current are effectively zero.

Total energy loss

Eq's (8-5) and (8-8) give the total energy loss in R_3 during this state of operation:

$$E_{\Sigma} = E_{R01} + E_{R12} = \frac{RI_O^2}{4}(2C\frac{V_{DC}}{I_O} - CR) + \frac{1}{8}C(R^2 I_O^2) \qquad (8\text{-}11)$$

If R_O is defined as:

$$R_O = \frac{V_{DC}}{I_O} \qquad (8\text{-}12)$$

then Eq. (8-11) can be written as:

$$E_{\Sigma} = [\frac{R}{R_O} - (\frac{R}{2R_O})^2]\frac{1}{2}CV_{DC}^2 \qquad (8\text{-}13)$$

where $\frac{1}{2}CV_{DC}^2$ is the energy which was stored in C_3 at $t = t_0$.

If the term between brackets is equal to 1, then all of the energy stored in C_3 will be dissipated in R_3, at which time the snubber resistor can be calculated from:

$$\frac{R}{R_O} - (\frac{R}{2R_O})^2 = 1 \qquad (8\text{-}14)$$

which gives:

$$R = 2R_O \qquad (8\text{-}15)$$

At this value of snubber resistor, all the energy stored in C_3 will be dissipated in R_3 when Q_2 and Q_4 are turned "off", which is the maximum energy dissipation in R_3 during this period.

To show how the energy loss is changed with R, the normalised energy can be defined from Eq. (8-13) as:

$$E_N = \frac{E_\Sigma}{\frac{1}{2}CV_{DC}^{\ 2}} = \frac{R}{R_O} - (\frac{R}{2R_O})^2 \qquad (8\text{-}16)$$

Fig. 8-20 shows how the normalised energy changes with R/R_O , which shows that when $R = 2R_O$, the normalised energy equals 1.

8-9-4 Q_1 and Q_3 Turn-On

When Q_1 and Q_3 turn "on", no change in the previous state occurs since the freewheeling diodes conduct the complete load current, unless the current is small such that the voltage drop across the switches (if MOSFET's) is smaller than the threshold voltage of the diode. In this case, the MOSFET's conduct the load current but in the opposite direction, i.e. from the source to the drain inside the MOSFET .

8-9-5 Q_1 and Q_3 Turn-Off

Also there is no change in the previous state if the diodes were conducting the load current. If the MOSFET's were conducting, the current will simply be diverted to the freewheeling diodes.

8-9-6 Q_2 and Q_4 Turn-On

When Q_2 and Q_4 are turned "on" again, the right half of the bridge looks like that shown in Fig. 8-18c, where Q_4 is replaced by a short circuit. In this case, V_X will be V_{DC}, C_4 discharges through the short circuit and R_4, while C_3 charges through R_3. The current in R_3, which is the charging current, is found to be given by:

$$i_S = \frac{V_{DC}}{R} e^{-t/(RC)} \qquad (8\text{-}17)$$

The energy loss in R_3 in this case is:

$$E_{R3} = R\int i_S^{\,2}\,dt = R(\frac{V_{DC}}{R})^2\int e^{-2t/(RC)}dt$$

$$E_{R3} = \frac{V_{DC}^{\,2}}{R}(-\frac{RC}{2}e^{-2t/(RC)})_{0\to\infty} = \frac{1}{2}CV_{DC}^{\,2} \qquad (8\text{-}18)$$

which is the same energy stored now in C_3.

8-9-7 Sizing the Power of the Snubber Resistor

The total energy lost in one complete cycle in R_3 is given by combining Eq's (8-13) and (8-18) which yields:

$$E_{TOT} = [1+\frac{R}{R_O}-(\frac{R}{2R_O})^2]\frac{1}{2}CV_{DC}^{\,2} \qquad (8\text{-}19)$$

where R_O is given in Eq. (8-12).

The power dissipation due to this energy is:

$$P_{TOT} = f_{SW}E_{TOT} = [1+\frac{R}{R_O}-(\frac{R}{2R_O})^2]\frac{1}{2}CV_{DC}^{\,2}f_{SW} \qquad (8\text{-}20)$$

For example, the circuit shown in Fig. 8-17 was practically examined with the following parameters:

f_{SW} = 20 kHz, C = 2.2 nF, R = 10 Ω, V_{DC} = 300 V, I_O = 5 A, and R_O as given in Eq. (8-12) is R_O = 60 Ω.

The power loss in each snubber resistor according to Eq. (8-20) is:

$$P_{TOT} = [(1+\frac{10}{60}-(\frac{10}{120})^2]\frac{1}{2}\cdot 2.2\cdot 10^{-9}(300)^2\cdot 20\cdot 10^3 \approx 2.3\ \text{W}$$

The snubber resistor has been increased from 10 Ω to 18 Ω to reduce the peak charging current to acceptable levels. The power dissipation now became about 2.5 W, and the resistor temperature has increased.

If R is increased to $2R_O$ = 120 Ω as described earlier, then the maximum power dissipation can be calculated to be about 4 W.

8-9-8 Circuit Simulation

Fig. 8-21 shows the circuit used to simulate the full-bridge circuit of Fig. 8-17, where Fig. 8-21a simulates the turn-off of Q_2 and Q_4, while Fig. 8-21b simulates the turn-on.

Fig's 8-22 and 8-23 show different voltage, current and energy waveforms for the simulated example that has the same parameters as the practical circuit, for different values of snubber resistors, 10, 18 and 120 Ω. The first two values are the ones used in the practical circuit, while the latter one is the value corresponding to $2R_O$.

Fig. 8-22a shows that when $R < 2R_O$,the current in the snubber is $I_O/2$ before the diode conduction, and then decreases exponentially at a time constant RC. At R = $2R_O$ (120 Ω), the current decreases exponentially right from the beginning.

Fig. 8-22b shows the voltage across the snubber capacitor, where it is seen the linear decrease before the diode conduction as given in Eq. (8-1), and then the exponential decrease after the diode conduction as given in Eq. (8-6). Also noticed is that this voltage is $RI_O/2$ at the instant of diode conduction. When $R = 2R_O$ = 120 Ω, $\Delta t = 0$ as given in Eq. (8-4), and the voltage decreases exponentially from the beginning.

Fig. 8-22c shows the dissipated energy in the snubber resistor, where it is seen that when $R = 2R_O$, the dissipated energy is the same as the stored energy in the capacitor (99 μJ in the simulated example).

Fig. 8-23 shows the same waveforms at Q_2 and Q_4 turn-on. The dissipated energy (Fig. 8-23c) is now the same as the stored energy in the capacitor as given in Eq. (8-18), and does not depend on the resistor value.

Needless to say that the energy dissipated in all snubber resistors are equal during one complete cycle, irrespective of the direction of the load current.

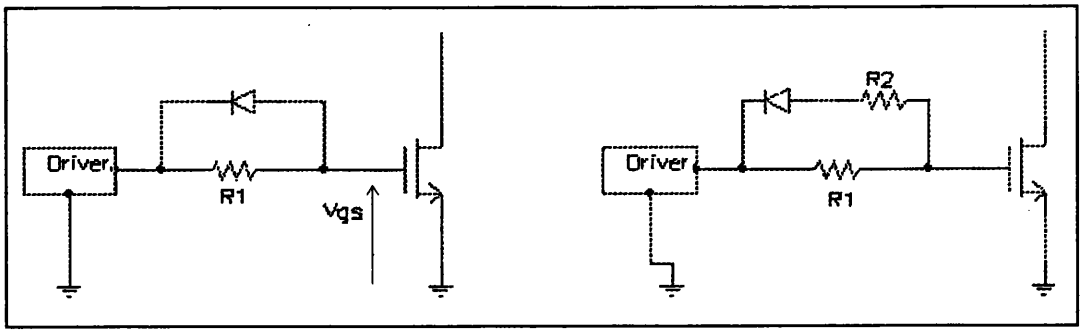
Fig. 8-24 shows photographs for the practical PWM full-bridge dc/ac inverter together with the test set-up.

8-10 CONCLUSION

Circuit layout is a critical issue in the design of full-bridge dc/ac inverters. If this is taken into consideration, stray inductance can be reduced, which has the effect of allowing lower snubber capacitor values to be used. This in turn reduces the MOSFET peak current at turn-on which reduces switching loss and keeps the MOSFET within the safe operating area. Reducing stray and leakage inductance can also reduces the voltage spike at turn-off, which further allows for lower snubber capacitor values and reduces the switched VA.

Using resistor/diode pairs for creating dead time is not recommended for inductive loads, as it increases the turn-off speed which is the main cause of MOSFET failure.

Placing the output filter at the primary side, has the effect of considerably reducing the output high frequency noise due to transformer interwinding capacitance and reduces transformer losses.



(a) (b)

Fig. 8-1 Circuit arrangements to create the dead time

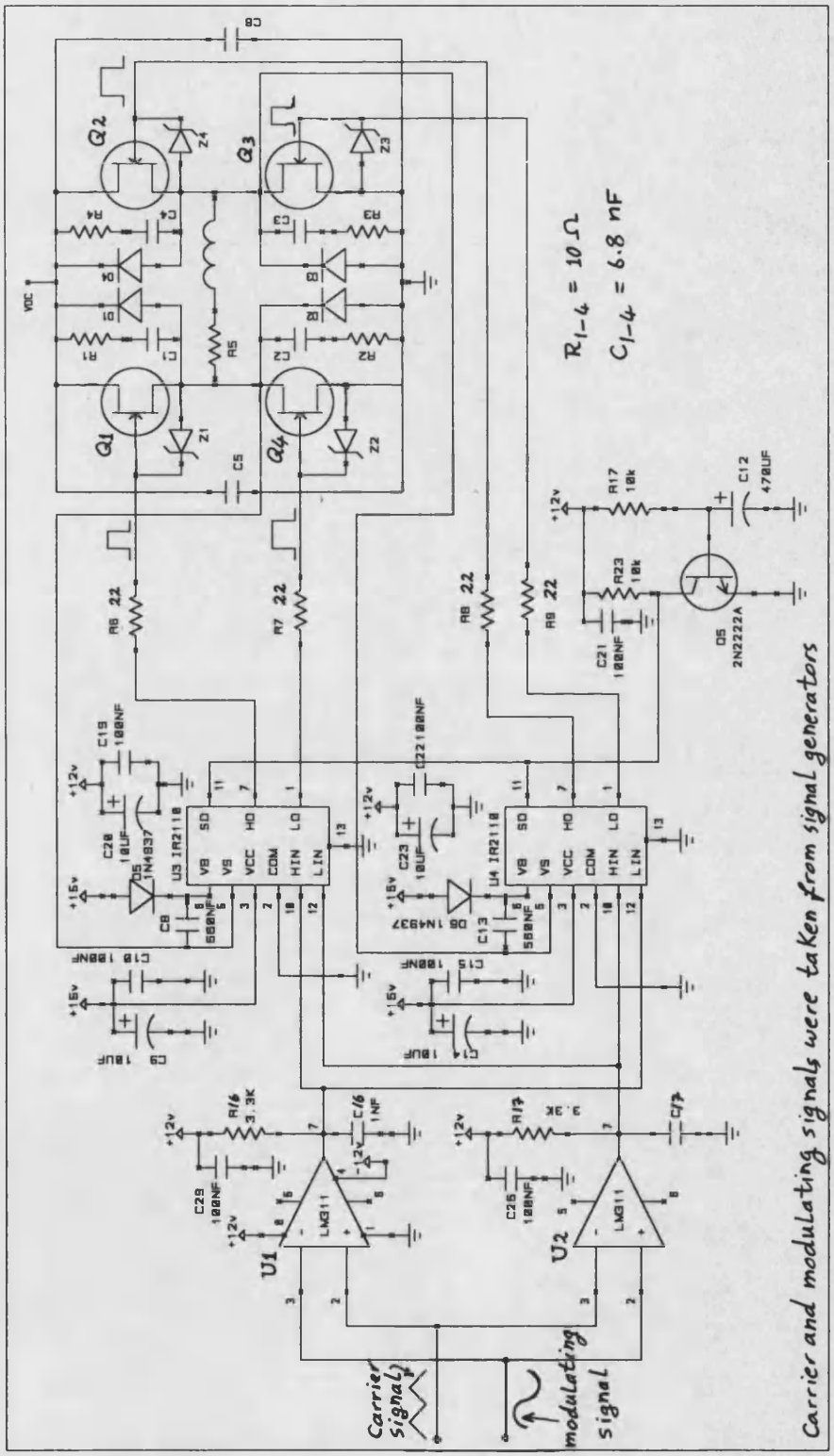


Fig. 8-2 The practical full-bridge dc/ac inverter

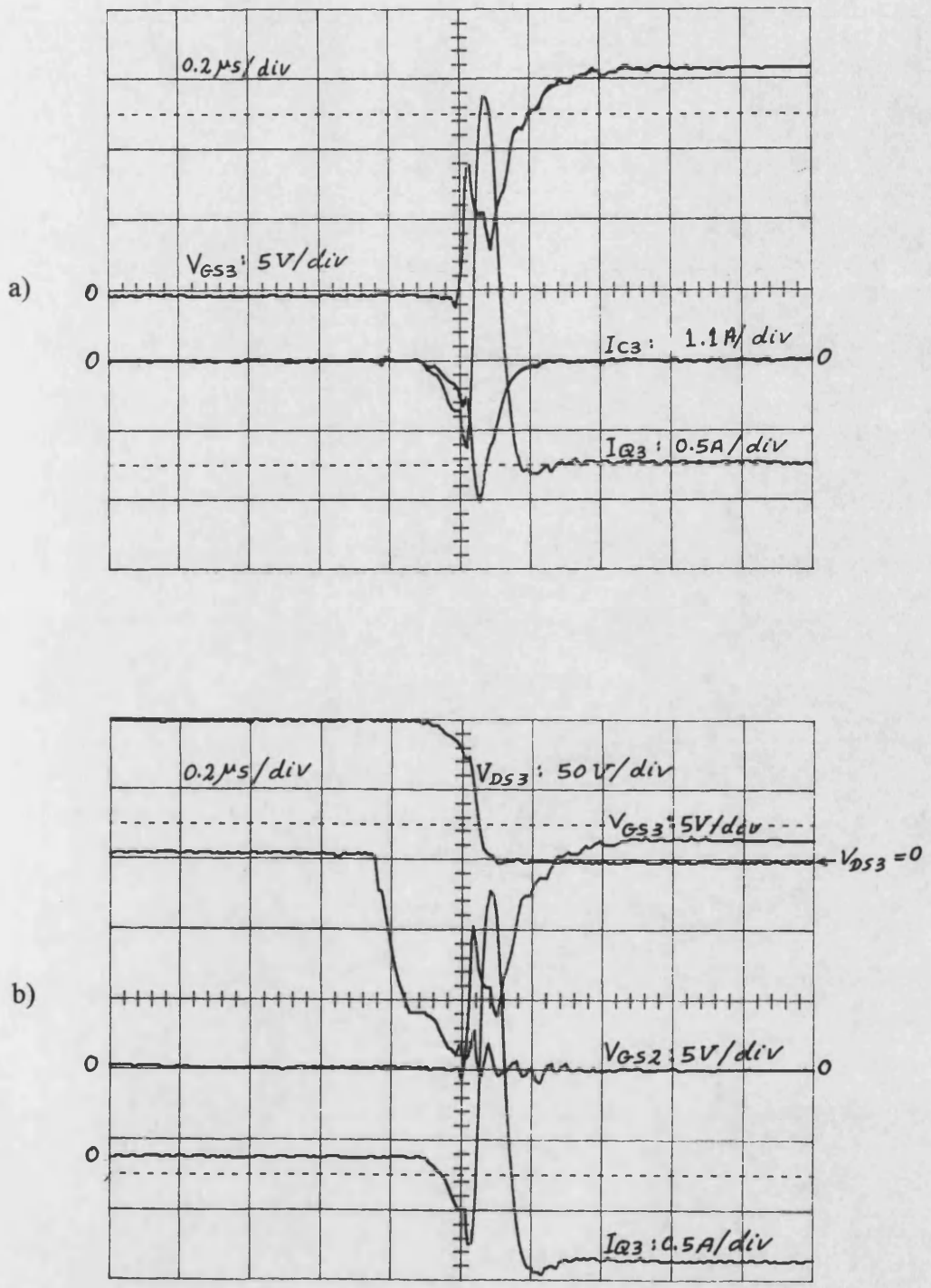
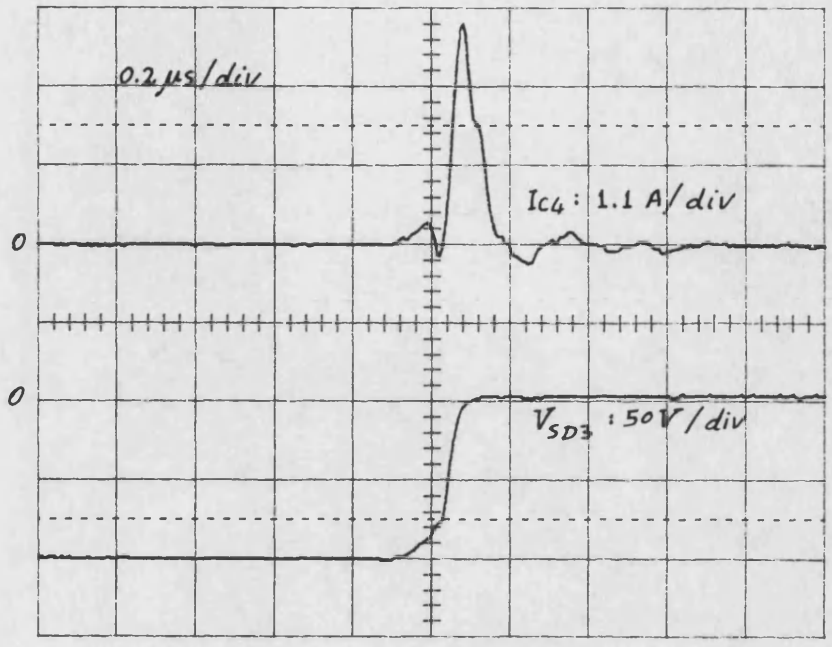


Fig. 8-3 Practical waveforms for the inverter shown in Fig. 8-2 at turn-on: V_{DC}=100V, dead time=0.4μs

c)



d)

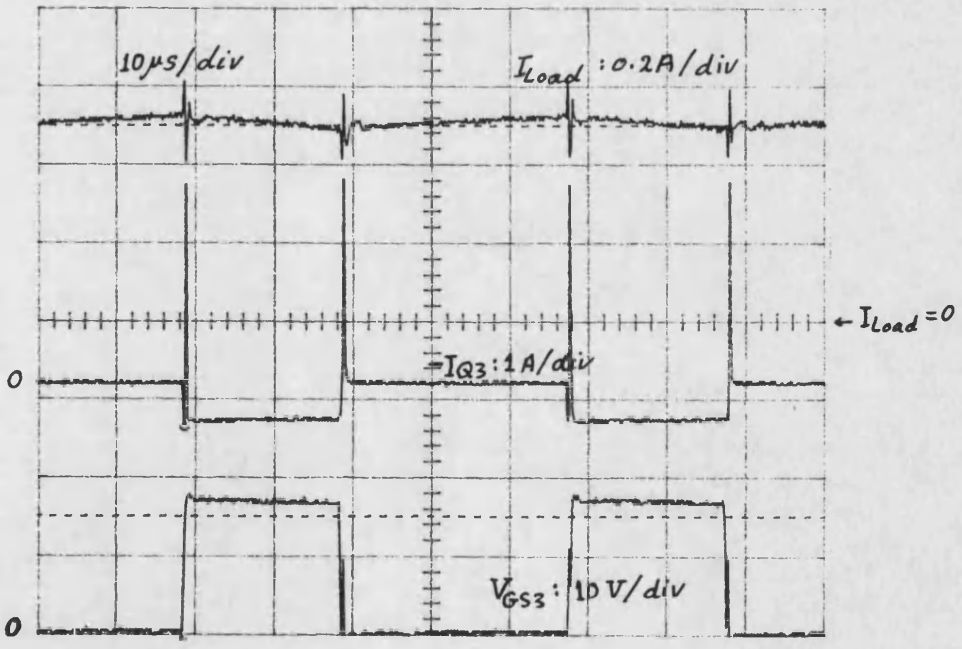


Fig. 8-3 c) Snubber current, I_{C4}, of the upper branch and d) complete waveforms

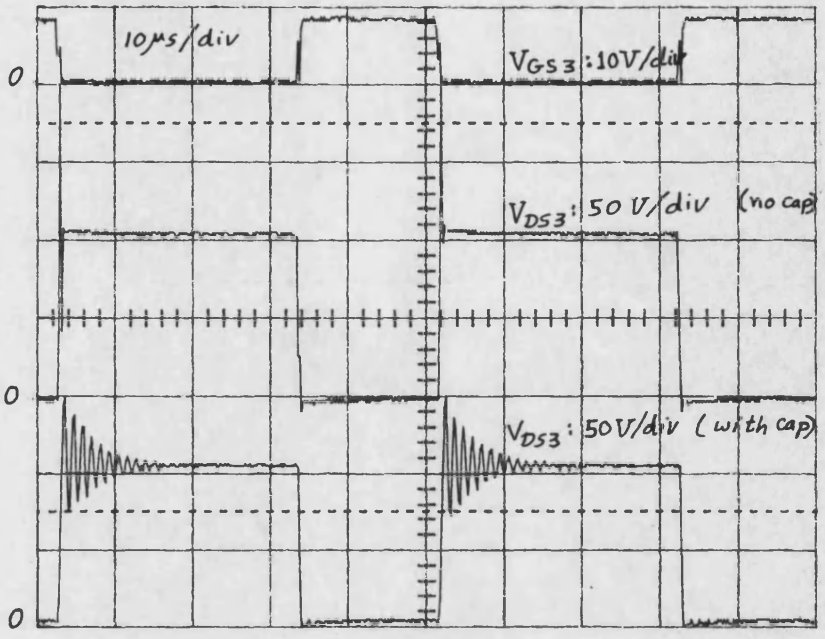


Fig. 8-4 The complete practical waveforms using IRFP450

a)

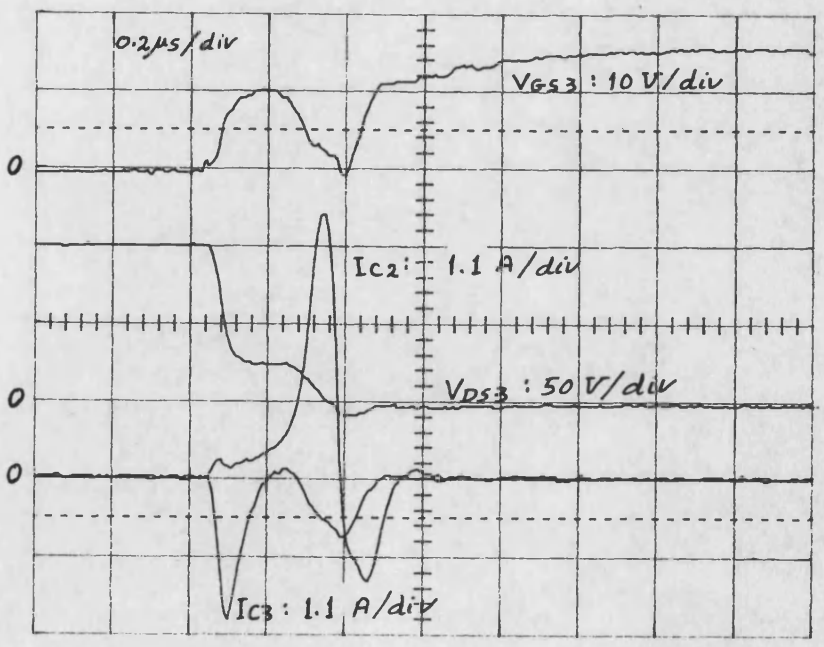


Fig. 8-5 a) Turn-on waveforms using IRFP450 without decoupling capacitors

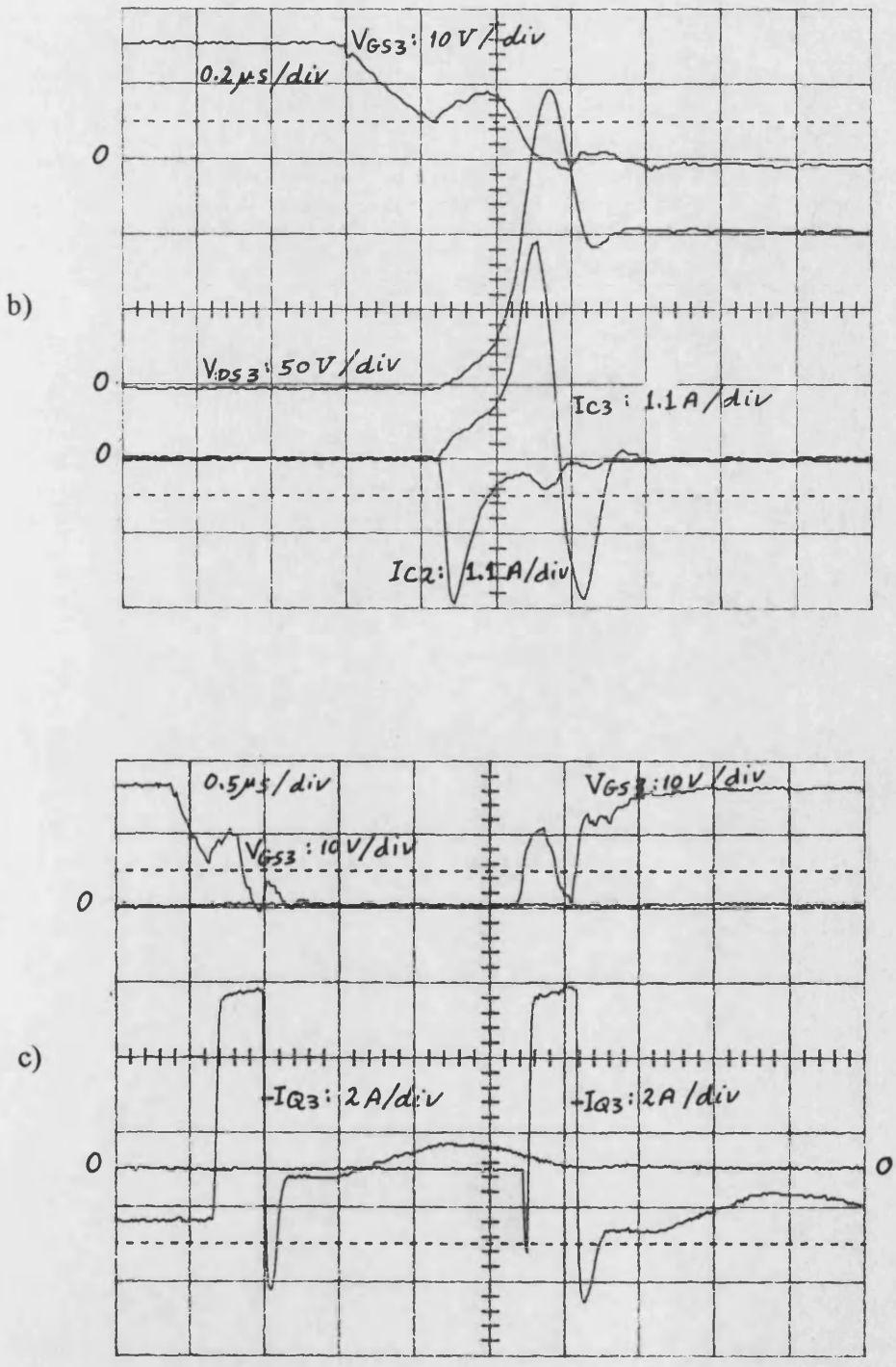


Fig. 8-5 b) Turn-off waveforms and c) turn-on and turn-off switch currents using IRFP450 without decoupling capacitors

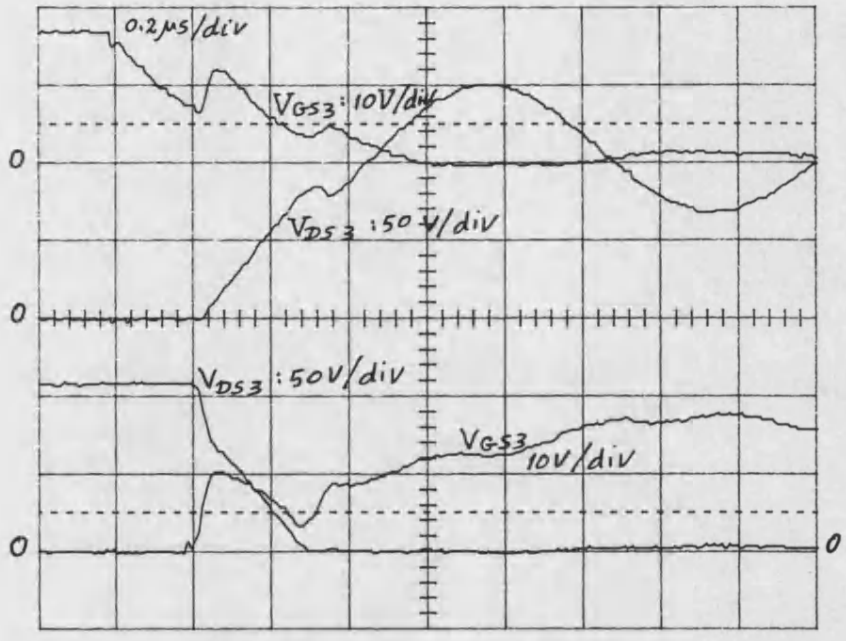


Fig. 8-6 Turn-on and turn-off waveforms with decoupling capacitors

a)

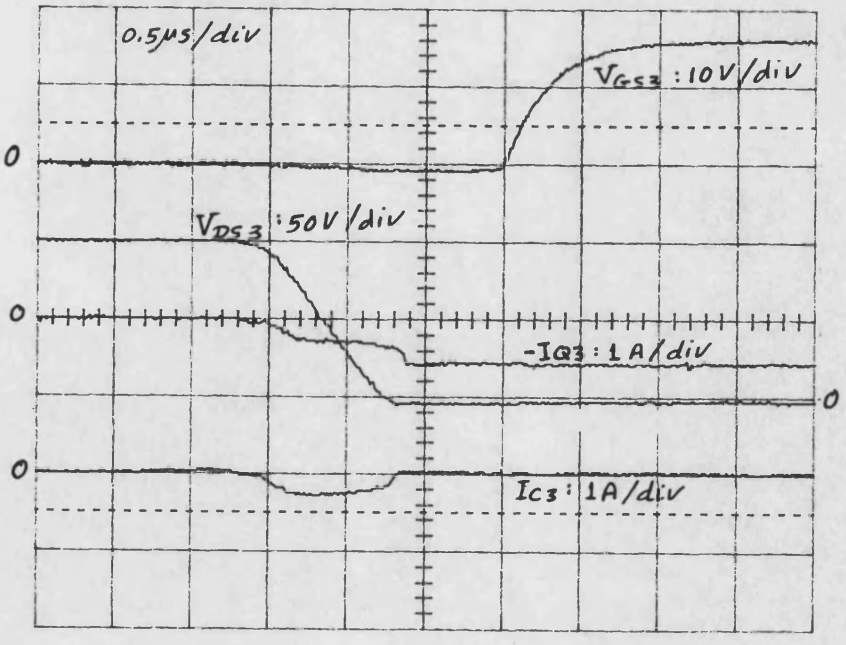
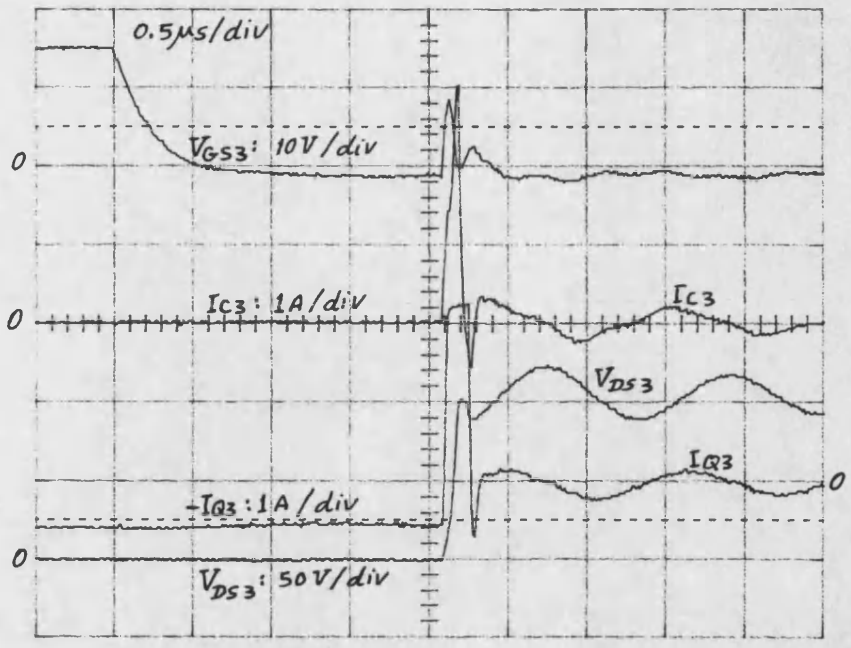


Fig. 8-7 a) Turn-on waveforms after increasing the dead time to 2.1μs

b)



c)

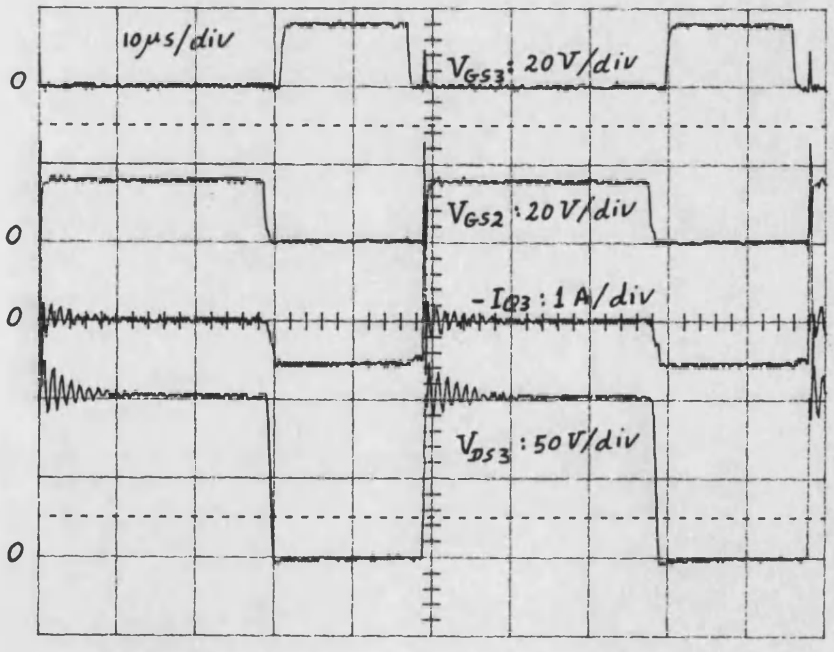


Fig. 8-7 b) Turn-off and c) complete waveforms after increasing the dead time to 2.1μs

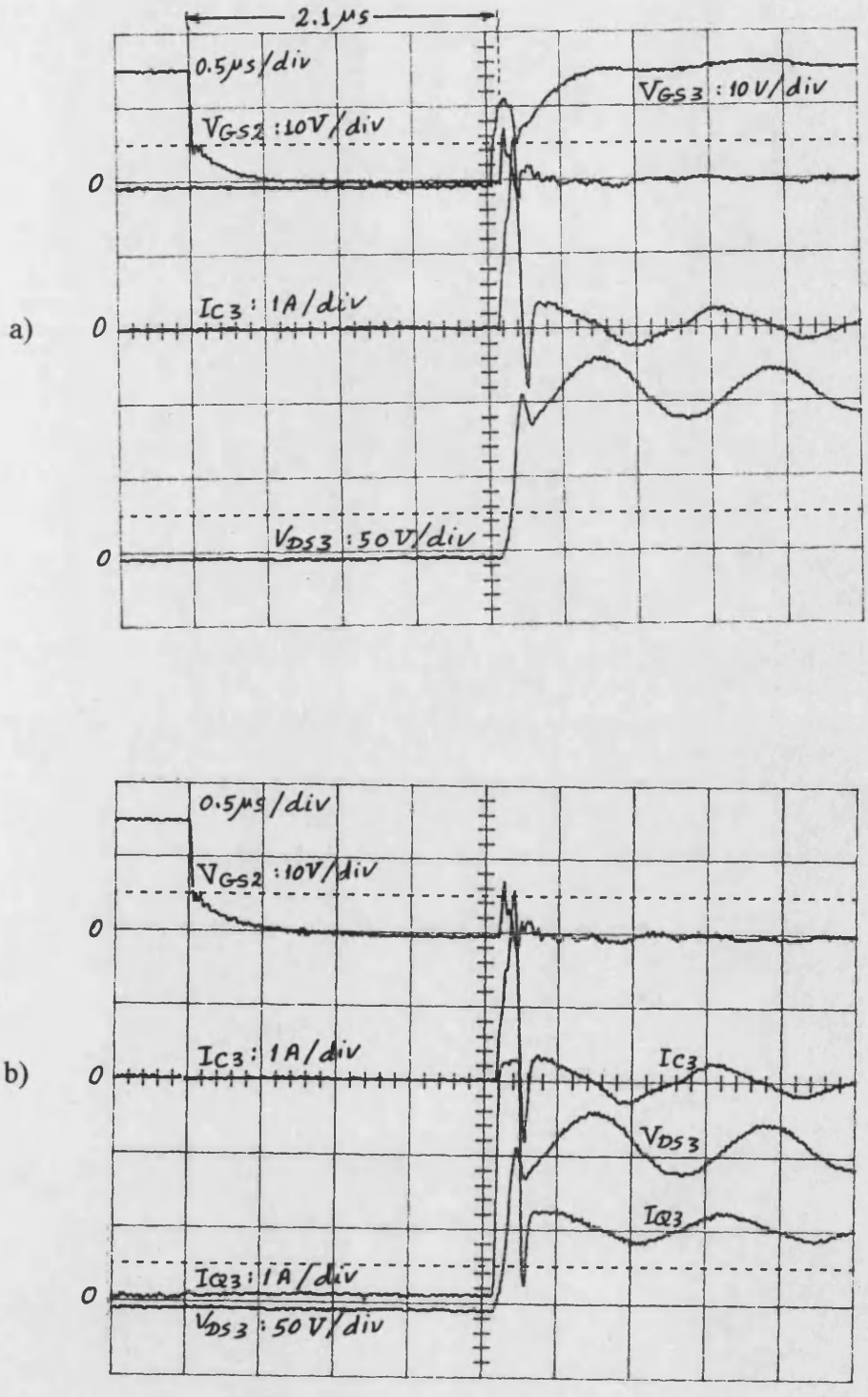
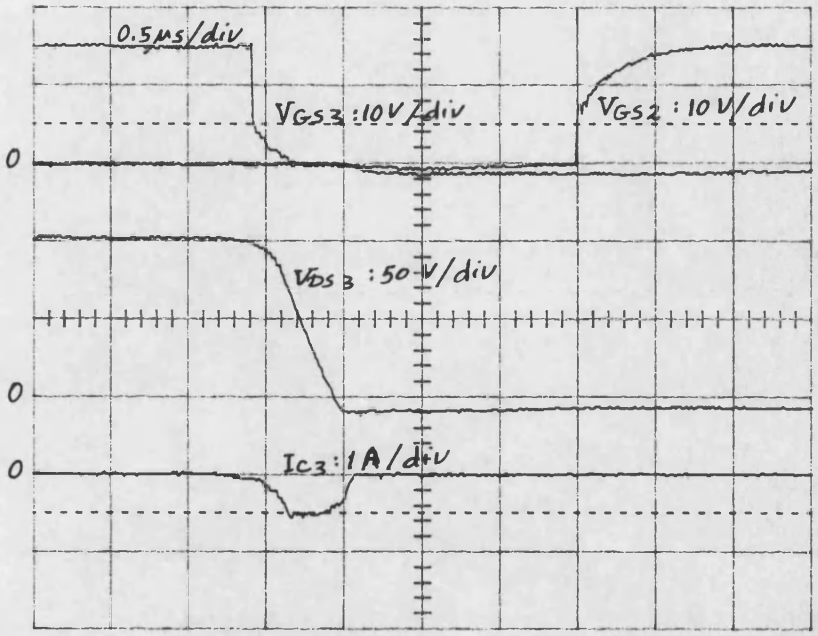


Fig. 8-8 Turn-on waveforms after reducing the gate-circuit inductance

c)



d)

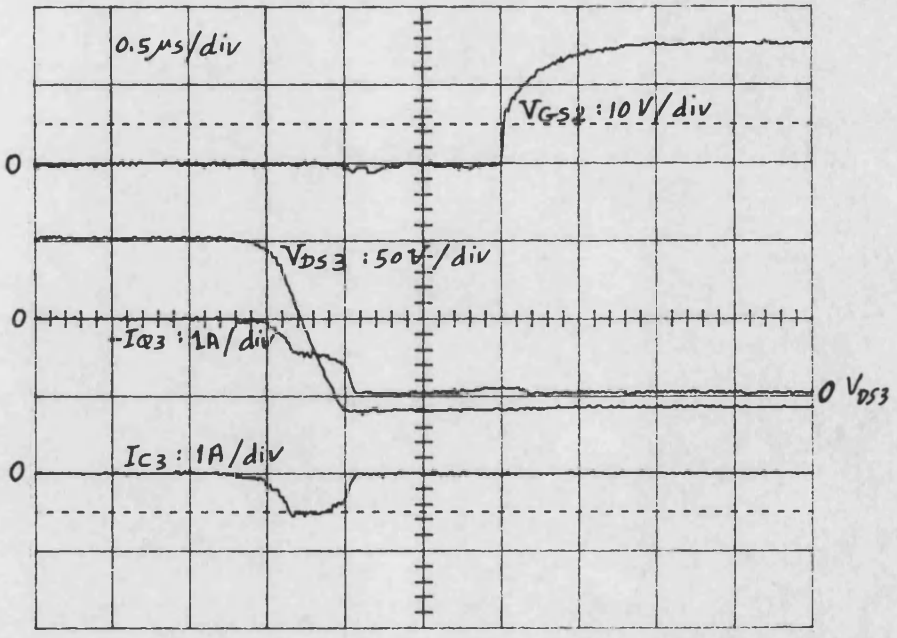
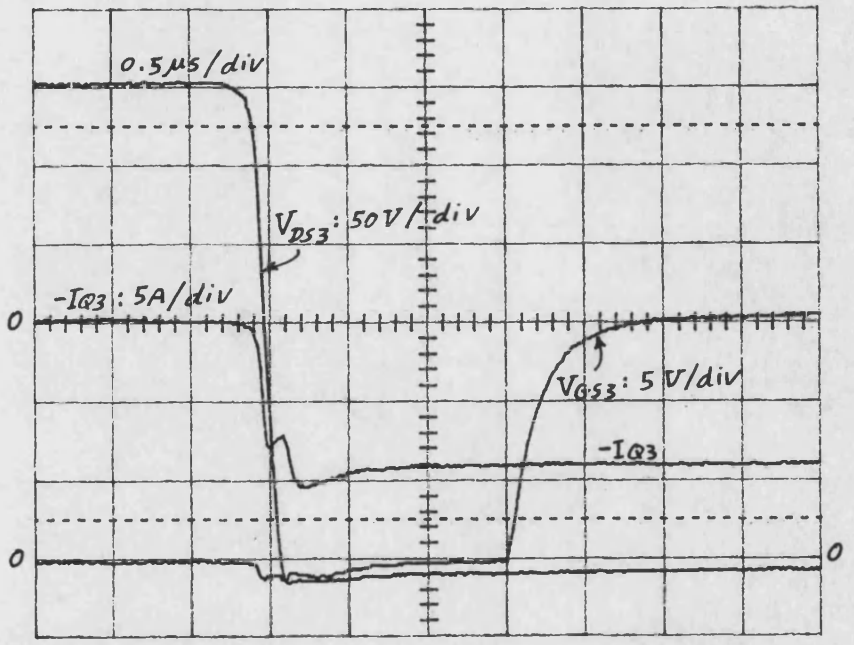


Fig. 8-8 Turn-off waveforms after reducing the gate-circuit inductance

a)



b)

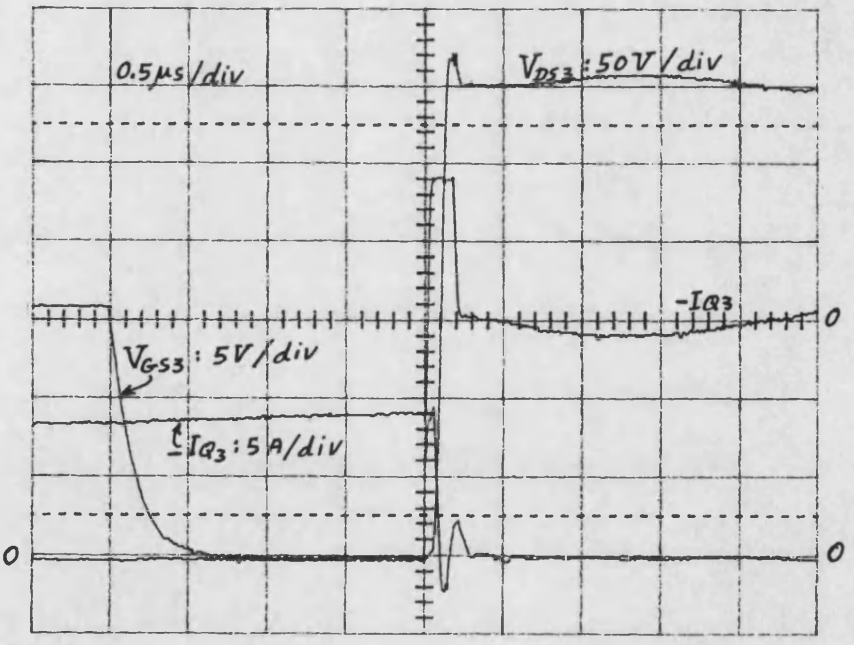


Fig. 8-9 a) Turn-on and b) turn-off waveforms after increasing the value of decoupling capacitors from 100n to 470n: V_{DC}=280V, I_{AV}=5.5A, I_{PK}=8A

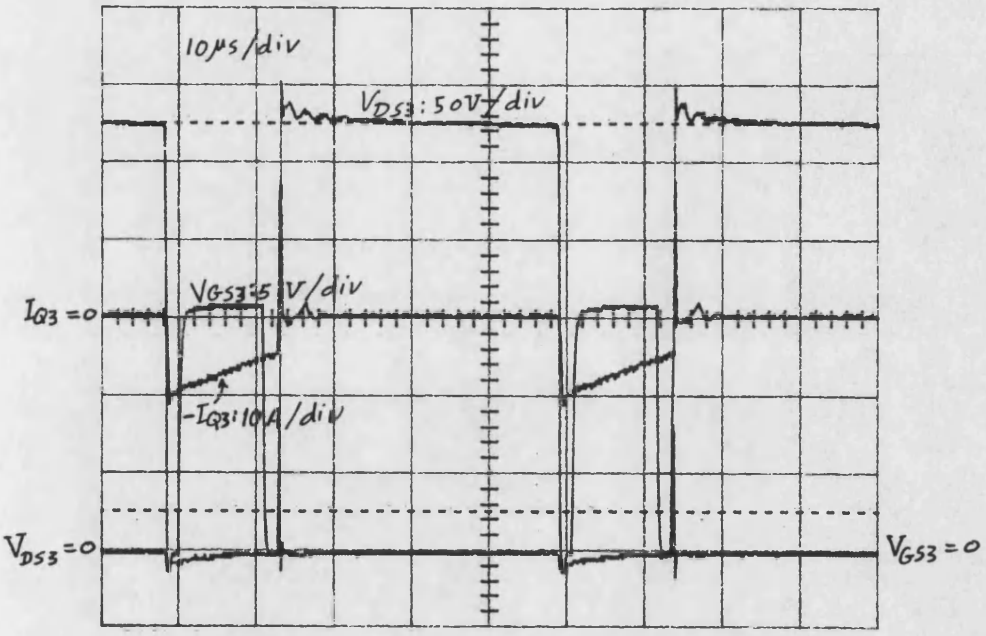


Fig. 8-9 c) The complete waveforms of V_{GS3}, V_{DS3} and I_{Q3}

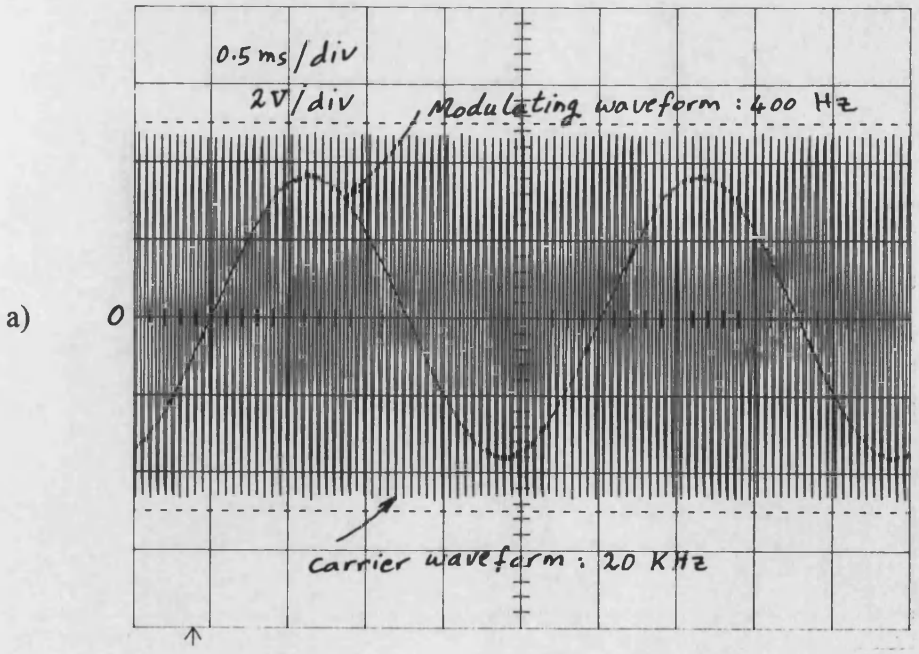


Fig. 8-10 a) Carrier and modulating waveforms at the inputs of the comparator (see Fig. 8-2)

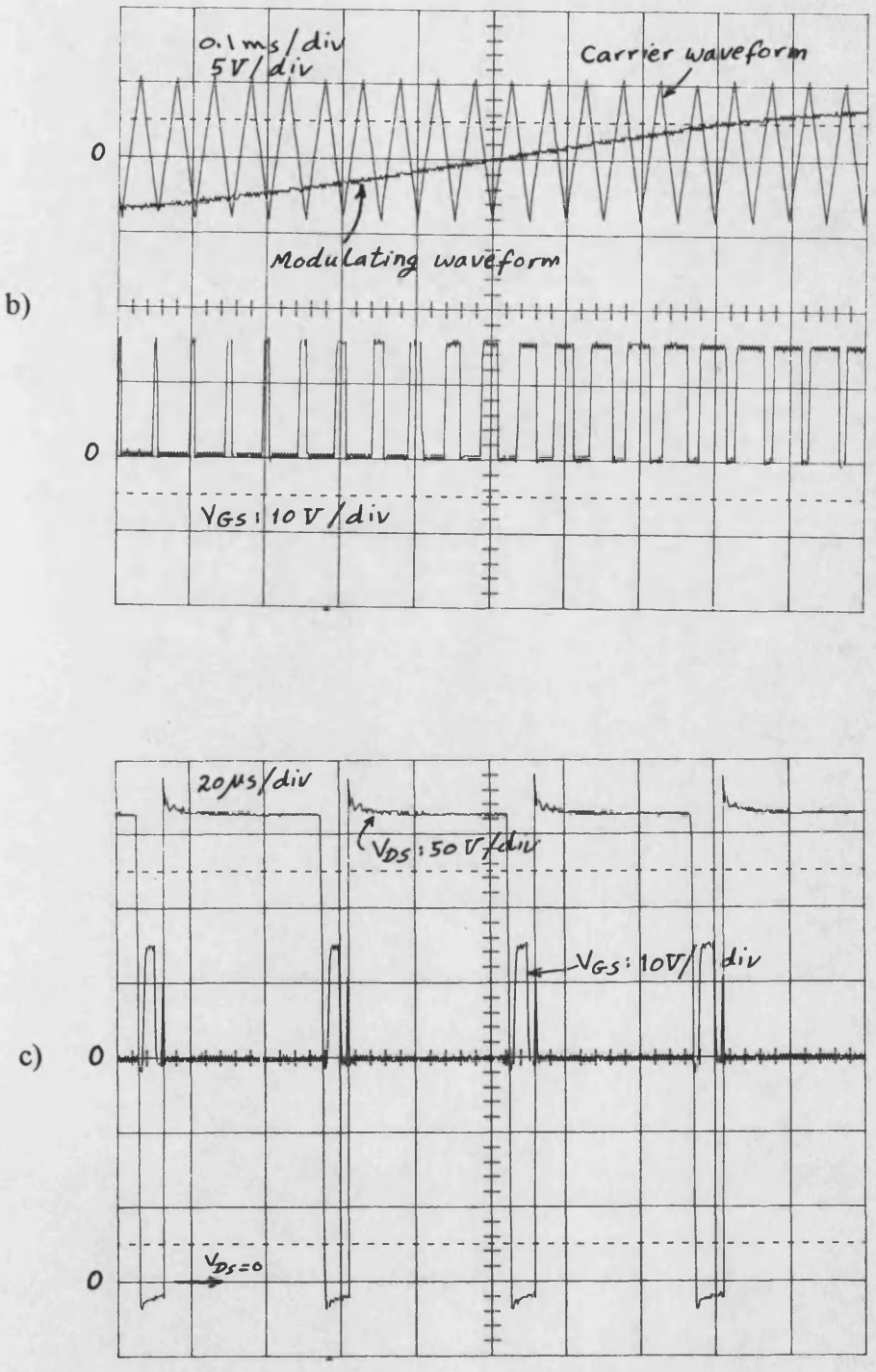


Fig. 8-10 Expanded waveforms: V_{DC}=320V

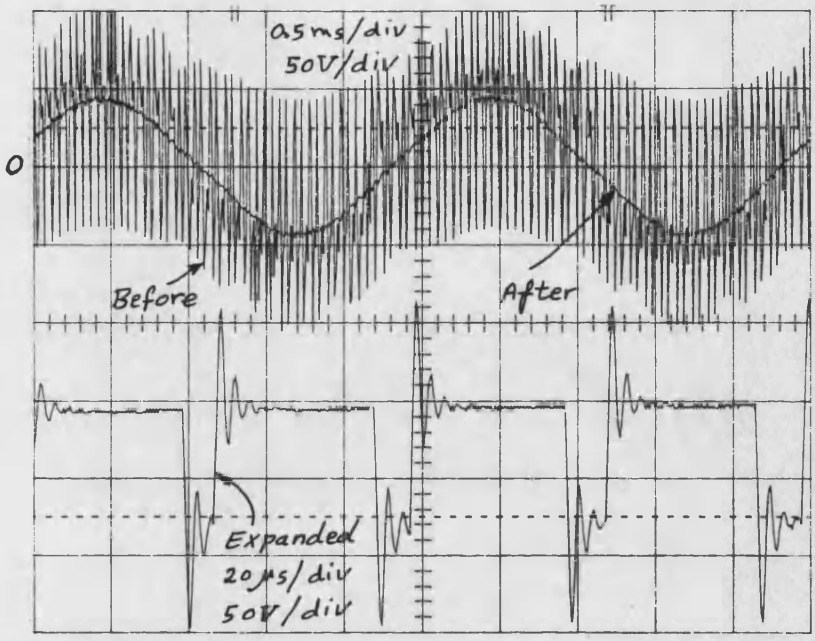


Fig. 8-11 The transformer secondary voltage before and after the output filter and expanded secondary voltage before the output filter

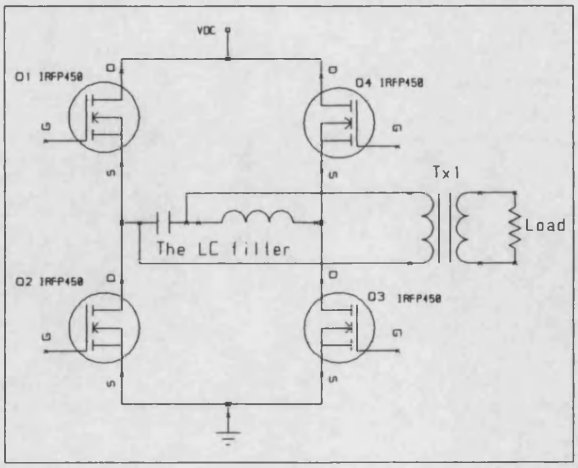


Fig. 8-12 Placing the filter at the primary side

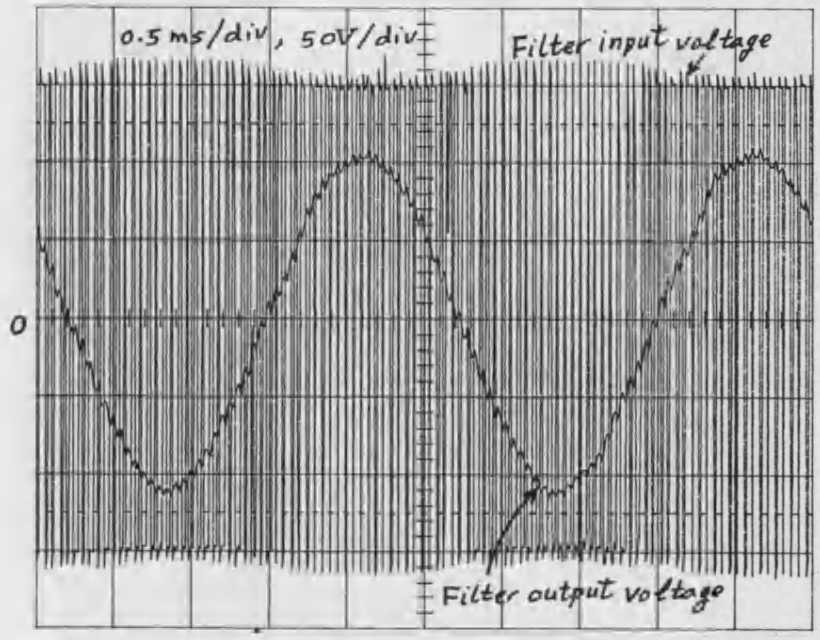


Fig. 8-13 Filter input and output voltages after placing it at the primary side

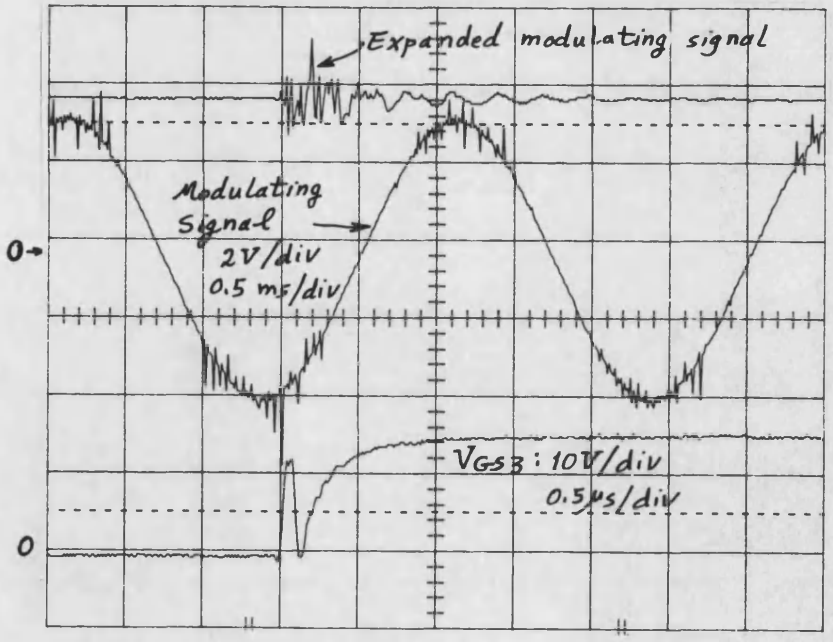


Fig. 8-14 The noise on the modulating signal (middle trace) caused by switching, expanded waveform (upper trace) and the gate-source voltage (lower trace)

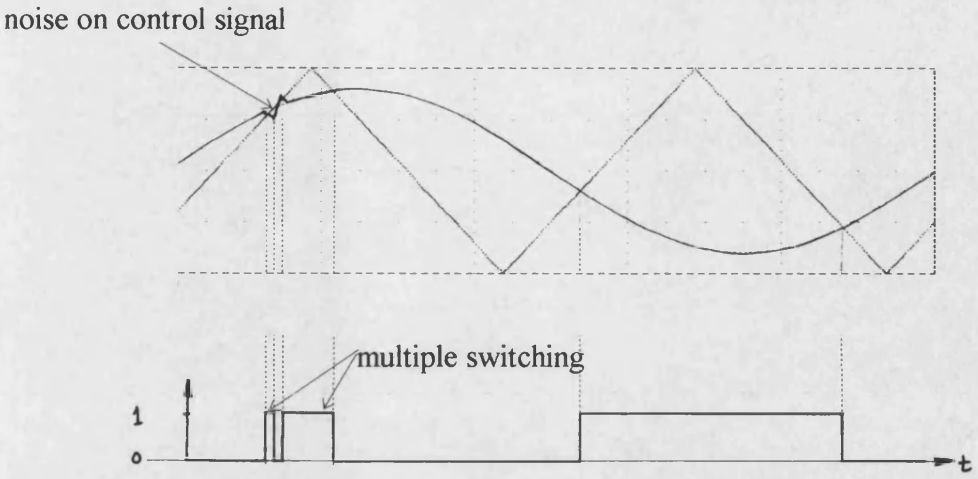
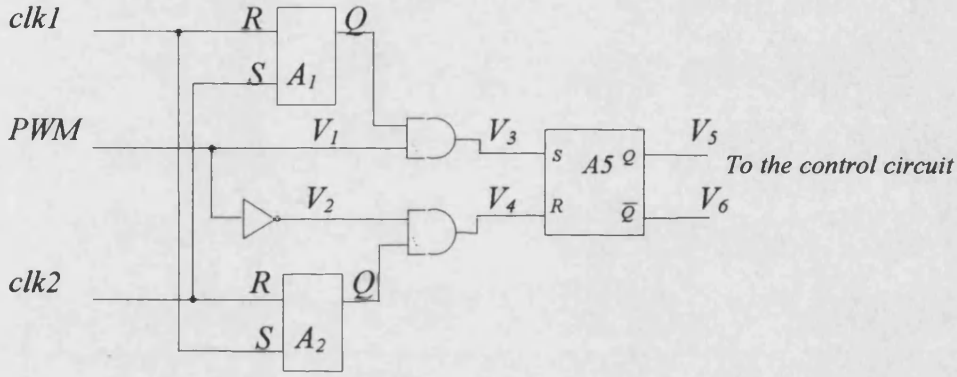


Fig. 8-15 Multiple switching caused by noise on the control signal

a)



b)

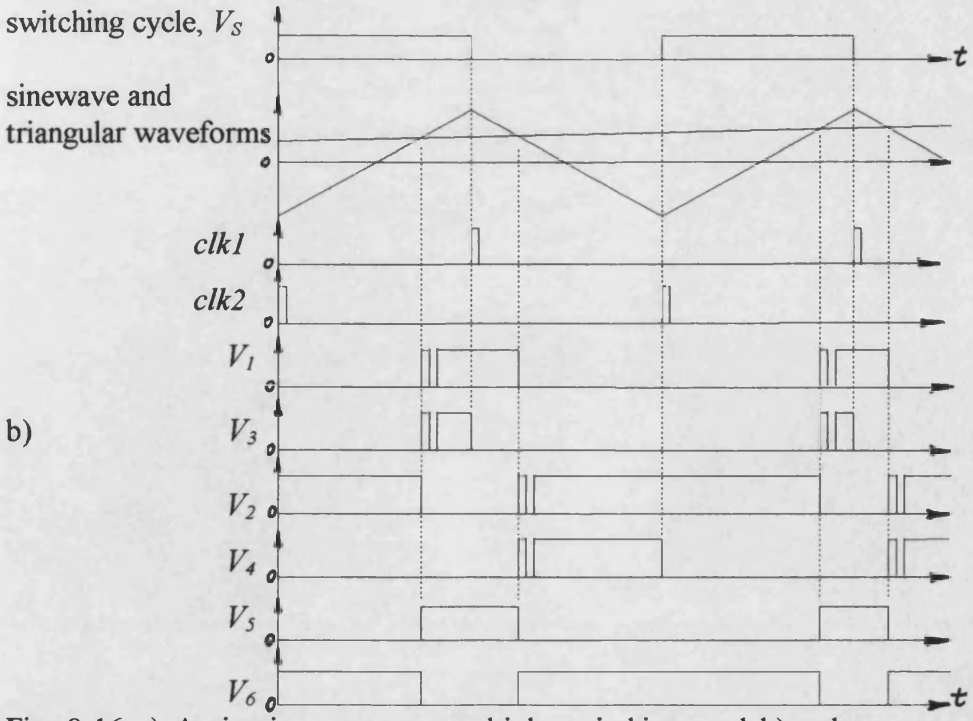


Fig. 8-16 a) A circuit to prevent multiple switching, and b) voltage waveforms in some points

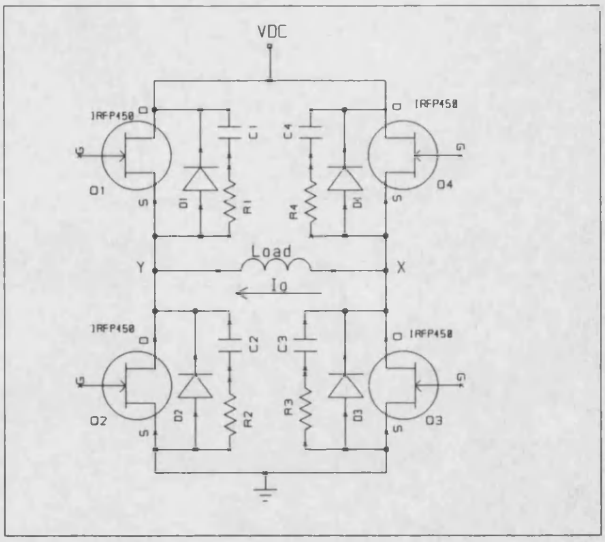
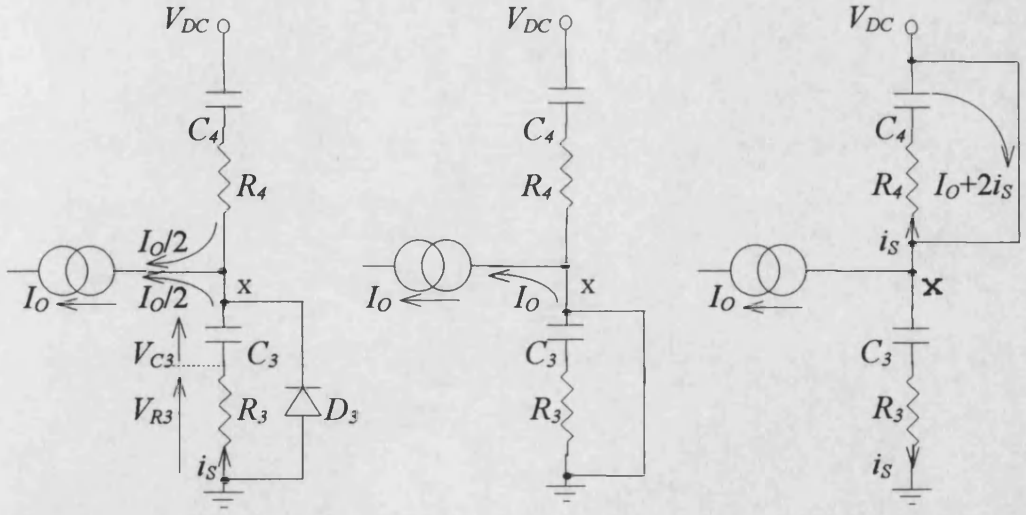


Fig. 8-17 The power stage of a full-bridge dc/ac inverter



a) Q_2 and Q_4 turn-off b) D_3 turn-on c) Q_2 and Q_4 turn-on

Fig. 8-18 Equivalent circuits at turn-on and turn-off of Q_2 and Q_4

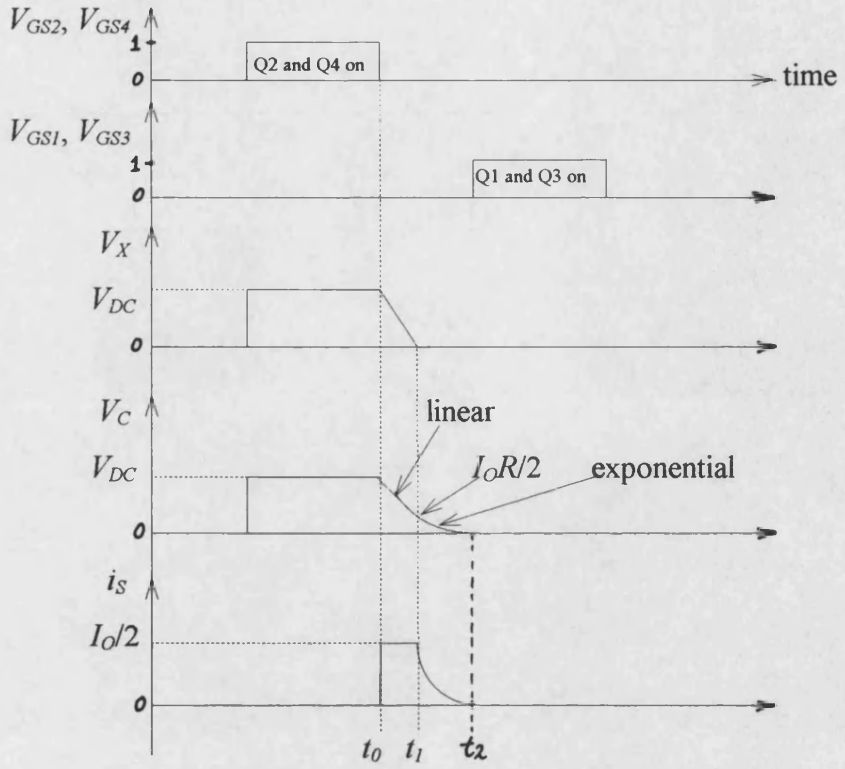


Fig. 8-19 Typical waveforms at Q_2 and Q_4 turn-on and turn-off

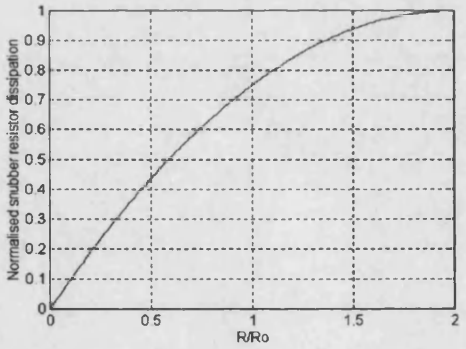
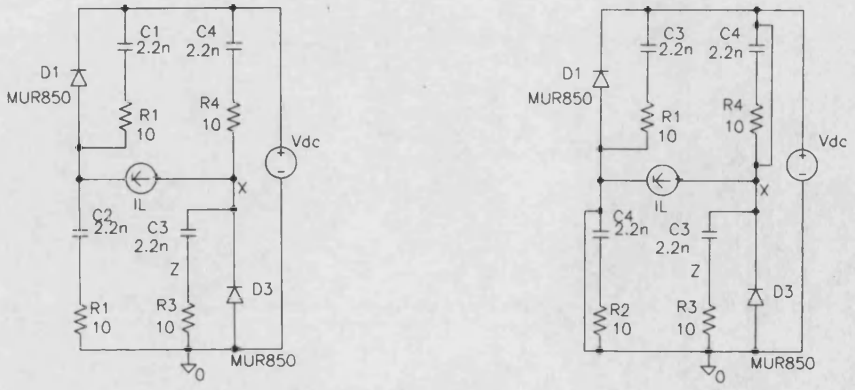
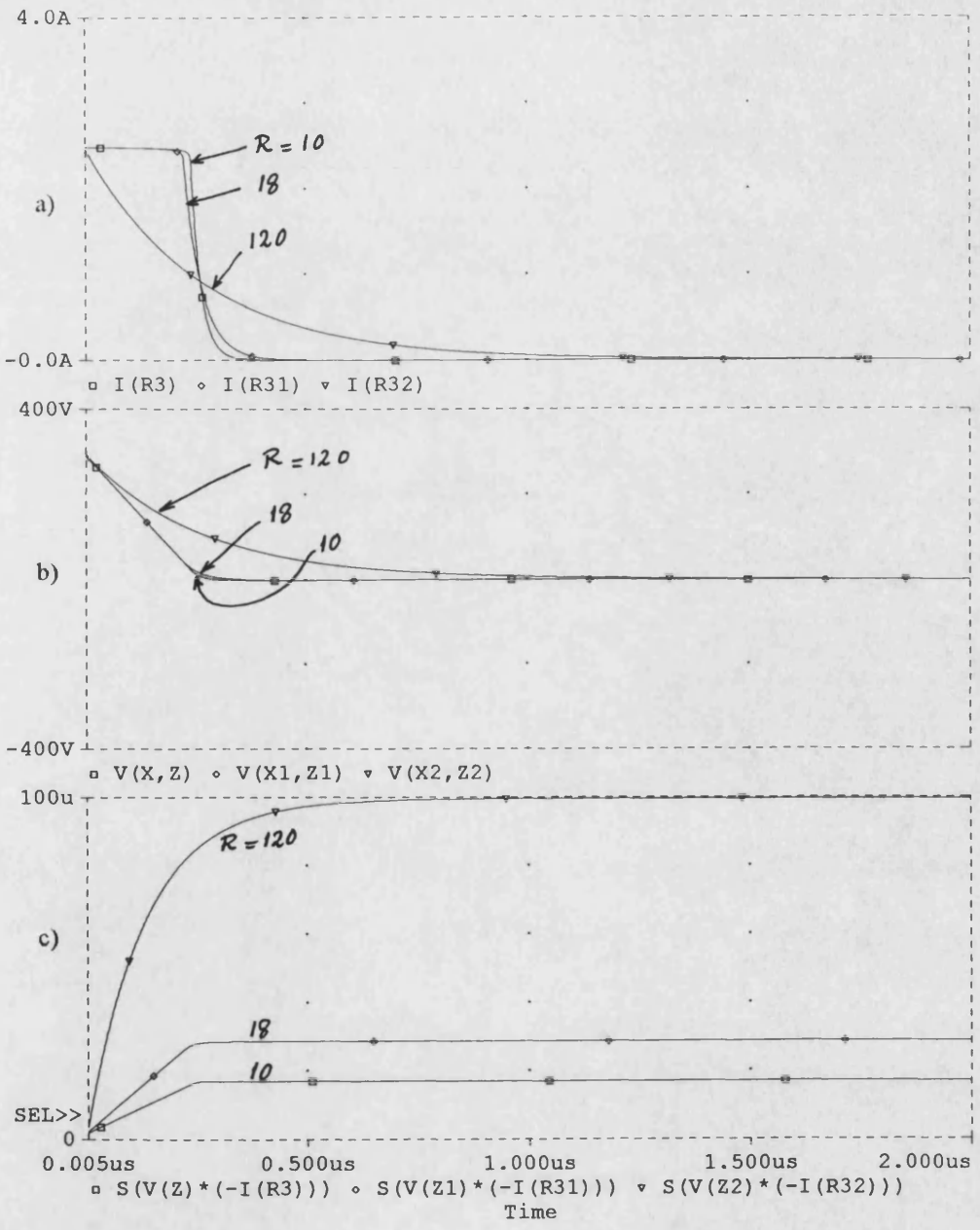


Fig. 8-20 The normalised energy dissipation in the snubber resistors



(a) (b)

Fig. 8-21 A circuit used to simulate a) the turn-off of Q_2 and Q_4 and b) the turn-on



Date: July 11, 1996

Fig. 8-22 a) voltage across the snubber capacitor, b) current in the snubber and c) energy dissipated in the snubber resistor during Q_2 and Q_4 turn-off

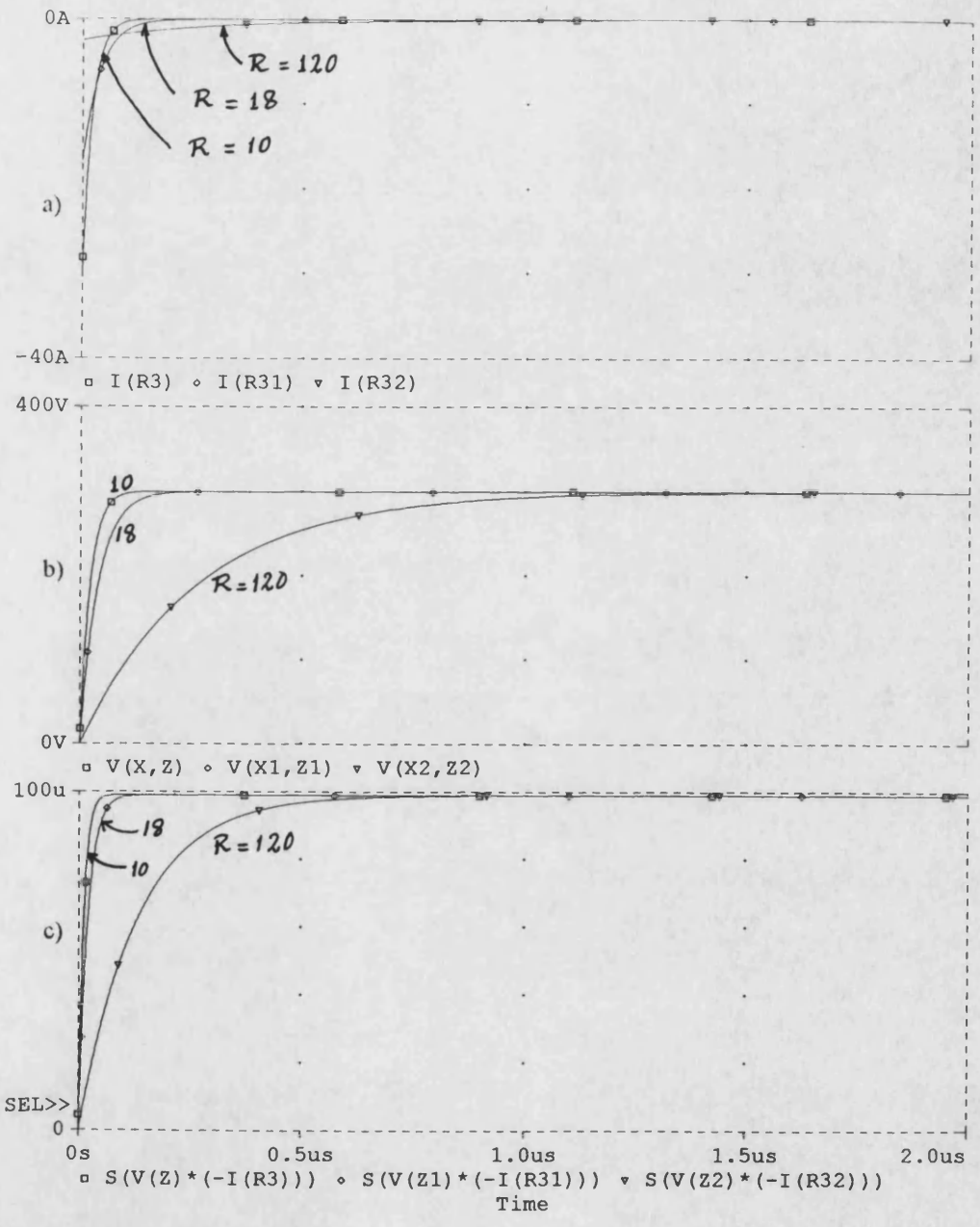
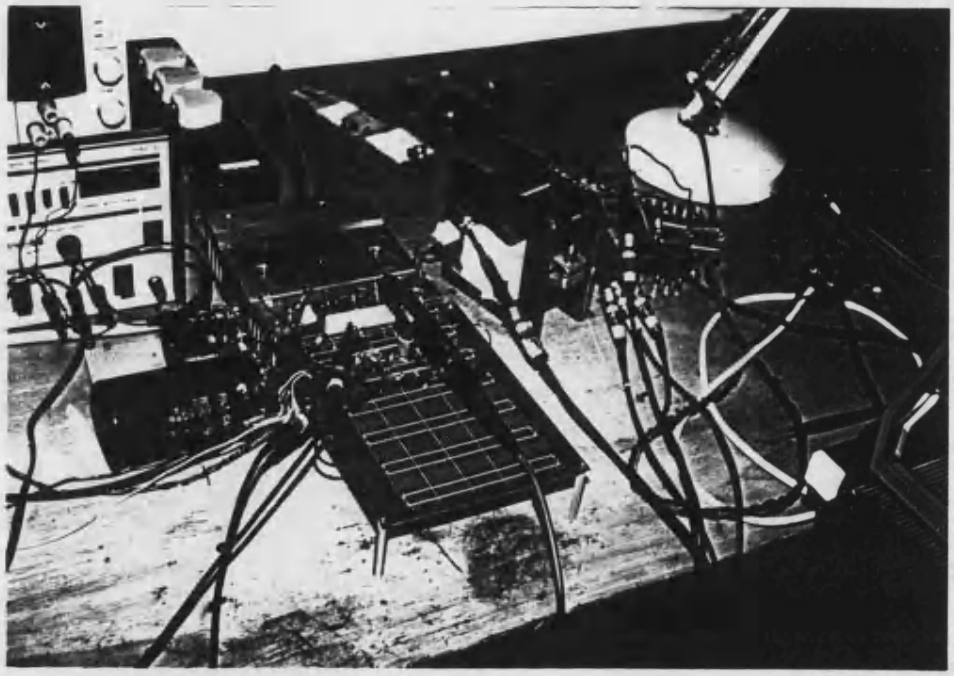


Fig. 8-23 a) voltage across the snubber capacitor, b) current in the snubber and c) energy dissipated in the snubber resistor during Q_2 and Q_4 turn-on

a)



b)

Fig. 8-24 Photographs for the practical PWM full-bridge dc/ac inverter with the test setup

CHAPTER EIGHT REFERENCES

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2. David L. Blackburn, "Turn-off failure of power MOSFET's", IEEE Transactions on Power Electronics, Vol. PE-2, No. 2, April 1987.
3. D. Grant, "HEXFET III: A new generation of power MOSFET's", Application Note 966A, International Rectifier.
4. Steve Clemente and Ajit Dubhashi, "HV floating MOS-gate driver IC", application note AN-978a, International Rectifier, USA, 1990.
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PARASITIC ELEMENTS IN POWER CONVERTERS

9-1 INTRODUCTION

Parasitic elements are undesirable passive component effects, usually caused by stray inductance and capacitance, which exist in electrical systems and have tremendous impact on the circuit behaviour. Their effect ranges from increasing power loss and output voltage ripple, to sometimes a catastrophic failure such as the destruction of the power devices, whether switches or rectifiers.

Component terminals and circuit interconnecting wiring, overlapping layers of material in semiconductor devices, wound tapes of material to produce capacitors and resistors produce this parasitic inductance and capacitance which is difficult to eliminate. This is especially true in power electronics circuits and components which must be relatively large to conduct and block high current and voltage, and absorb and conduct away significant power-loss.

The following sections briefly describe the main parasitic elements which the designer of switch-mode power supplies may encounter. The effect of these elements, ways to reduce their effect and methods to measure them are also presented.

9-2 LEAKAGE AND STRAY INDUCTANCE

9-2-1 Introduction

The first parasitic effect considered is transformer leakage inductance which, as its name indicates, is an undesirable inductance that exists in transformers due to a small amount of leakage flux that does not link to all turns of all windings. Fig. 9-1 shows an example where some of the flux lines are not linked to the other coil through the core, but close their path through air, and cause leakage inductance.

In comparison, useful flux is the flux that does link both windings of the transformer and induces voltage at the secondary, which is given by: $V = -N_S \, d\phi / dt$, where ϕ is the useful flux, and N_S is number of secondary turns. Usually, the inductance of an inductor is not exactly proportional to the square of the number of turns due to leakage inductance. The evidence of leakage inductance is that voltage transformation ratio is not exactly equal to the turns ratio. Another evidence is the existence of a small inductance in the primary when the secondary is shorted. Therefore, the equivalent circuit of a transformer requires two other inductances to represent the primary and the secondary leakage inductance, in addition to the magnetising inductance, L_M.

Leakage inductance is a distributed parameter, but practically it is simulated as a lumped element to simplify analysis of transformers. Leakage inductance has a considerable effect on transformers, especially at high frequencies, as will be shown later in this section.

Parasitic inductance due to wiring and component lead inductance is generally referred to as stray inductance. Connection wire and component lead lengths generally enclose larger areas in power electronics where components are bigger and less closely packed than in signal electronics.

In the following sections, parasitic inductance is used to describe both leakage and stray inductance, and is represented by L_L.

9-2-2 Ways of Reducing Parasitic Inductance

Leakage inductance can be reduced by reducing spacing between windings, increasing winding length, reducing number of turns, and decreasing the ratio of window-to-core area [1]. Leakage inductance can also be reduced by interleaving primary and secondary windings (though this increases the distributed capacitance), reducing number of layers and by arranging the primary and secondary windings concentrically [2, 3].

In push-pull applications, where the two halves of the primary have the same number of turns and the same wire diameter, leakage inductance can be reduced by using bifilar winding [3].

If an auto-transformer is used, leakage inductance can be reduced especially if the voltage ratio of the auto-transformer approaches unity. The greater the ratio, the lower the leakage inductance will be.

Leakage inductance is increased when screens are inserted in transformers because they occupy considerable space [3], and can be kept to a minimum if the transformers are wound on toroidal cores [4]. Therefore, many wide-band transformers are designed on toroids.

Stray wiring and component termination inductance is kept to a minimum by minimising the loop area enclosed by connecting wires and component leads. This is normally achieved by mounting components as close together as thermal and insulation requirement will allow, and by keeping current-supply and current-return wires as parallel as possible to and around the circuit.

9-2-3 Effects of Parasitic Inductance

Parasitic inductance, as magnetising inductance, stores energy when a current flows in the inductor. When the current is cut off, this energy ($1/2L_L i_P^2$) will be dissipated. Usually, this energy is dissipated in the power switch and resistive components as heat, and causes power loss and reduces efficiency. Even if techniques exist to return the stored energy to the supply line, the energy transfer is

not 100% efficient because power dissipation occurs in the steering diodes used in energy recovery circuits.

In addition to power loss, parasitic inductance can cause very high voltage spikes as in forward and flyback converters. The occurrence of voltage spikes necessitates the use of higher power switch and rectifier voltage ratings, which, in turn, increases the size and cost of the converter.

Fig. 9-2 shows a typical collector voltage waveform obtained in push-pull converters. When any of the power switches is turned "off", the current in the switch falls rapidly at a rate di_P / dt, causing a positive going spike at the collector of an amplitude $L_L di_P / dt$, where i_P is the primary current at the instant of cut-off. If L_L is high and/or the primary current through the switch changes rapidly, i.e. di_P / dt is high, very high spikes are induced which might cause avalanche breakdown and degrade or damage the power semiconductors.

Fig. 9-3 shows a typical collector voltage waveform for a single-ended forward converter with a prominent high voltage spike due to the parasitic inductance.

In principle, transformer leakage and magnetising inductance in double-ended forward, diagonal half-bridge flyback, push-pull half-bridge, and full-bridge converters, does not cause voltage spikes as in push-pull and single-ended forward converters because of the clamping diodes that clamp the voltage at only one or two diode drops above the supply line voltage. Hence the energy stored in the parasitic inductance is returned to the supply line and not lost (see Chapters 2 and 3 for more details on the effect of parasitic inductance in converters.) However, this is only true if the stray inductance in the freewheel diode to supply-reservoir-capacitor path is kept low so that transformer current may commutate to a low inductance reset path. Also some power loss occurs in clamping diodes and the reservoir capacitor and reduces the overall efficiency.

In MOSFET drivers, the parasitic inductance in the gate drive circuits, exhibits a high impedance for short transients and decouples the gate from its drive circuit. This frequently results in multiple switching in the MOSFET.

9-2-4 Measurement of Leakage and Stray Inductance

Leakage inductance can be measured by shorting the low-voltage winding and measuring the inductance of the high-voltage winding.

Stray inductance may be estimated by resonating it in switching circuits with a known good quality capacitor. The resonant frequency, f_O, is then measured and the stray inductance is calculated from the formula:

$$L_L = \frac{1}{C(2\pi f_O)^2} \tag{9-1}$$

Techniques are used to exploit the parasitic inductance as a part of the required inductance, as in resonant converters, since it is not possible to eliminate it completely.

9-3 MAGNETISING INDUCTANCE

9-3-1 Introduction

In transformers, the current transformation ratio $i_S / i_P = N_P / N_S$ is not exactly true. In practice, the primary current, i_P, consists of the reflected secondary current, $N_S / N_P \cdot i_S$ plus a magnetising current, i_M, used to produce the flux in the core. This current does not represent a power loss. It is used to maintain the magnetic field. Magnetising current lags the applied voltage by 90°. Therefore, it can be accounted for by an inductor in parallel with the ideal transformer as shown in Fig. 9-4. Any non-linear effects due to core material are represented by changes in this inductance.

The magnetising current arises from the finite permeability of practical core materials. Magnetising current, i_M, should be distinguished from no-load current or exciting current, I_O, which consists of i_M, plus another current, I_{LOSS}, that represents hysteresis

and Eddy-current losses in the core. This latter current is in phase with the applied voltage and can be accounted for by a pure resistance in parallel with the magnetising inductance as shown in Fig. 9-4. In fact, this resistance is not constant, but varies with the rate-of-change of the flux density, dB/dt; that is, it varies with the applied voltage.

The total current, I_O, can be measured by leaving the secondary circuit open, and measuring the primary current, which is the no-load current. Provided primary circuit impedance is low, magnetising inductance does not change with load variations since it reflects the properties of the core. However, it does change with flux density since it is proportional to μ, as shown in Fig. 9-5. Once the core is saturated, the permeability of the core reduces to that of air and equals to 1. The transformer behaves as if there is no core, or it has an air core.

Magnetising inductance is approximately the inductance seen looking into the primary with all secondaries open-circuited since primary winding leakage inductance is usually very much smaller.

Usually, the no-load current is less than 5% of the full primary load current (the secondary current reflected to the primary). The maximum permissible peak no-load current should be no greater than 10% of the primary load current.

The magnetising current, i_M, that flows in the primary, and the applied voltage v_P, are related by the formula:

$$v_P = (L_M + L_L) \cdot di_M / dt \tag{9-2}$$

Usually, L_L is small compared with L_M, Therefore, Eq. (9-2) can be written as:

$$i_M = \frac{1}{L_M} \int v_P dt \tag{9-3}$$

9-3-2 Effect of Magnetising Current

As noted earlier, the magnetising current, i_M, is necessary to produce the required flux since permeability is assumed to be finite. This current flows in the primary

circuit and does not cause power loss in the secondary circuit. On the other hand, i_M flows in the power switches and increases the primary power loss. Therefore, it has several drawbacks:

1. Causes additional heat in power switches and, therefore, in the system, with the negative consequences resulting from this heat.
2. Requires higher current ratings of power switches to accommodate for this extra current.
3. Must be reset, or cycled with zero average value, at the end of each switching cycle to prevent saturation.
4. Additional power-loss in 1. and 3. reduces the efficiency of the system.

Due to these drawbacks, magnetising current should be kept as low as possible.

9-3-3 Ways of Reducing Magnetising Current

Eq. (9-3) shows how i_M is related to L_M and v_P. Therefore, to keep i_M small, L_M should be large or v_P should be small. Usually, the applied voltage, v_P, is given by the application and can not be reduced. L_M, on the other hand, is the only parameter which can be used to reduce i_M. To find how L_M can be increased, some simple rules are followed:

$$H \cdot l_e = N_P \cdot i_M \tag{9-4}$$

where : H is the magnetic field strength [A/m],

l_e is the effective magnetic path [m],

N_P is the number of primary turns, and

i_M is the magnetising current [A].

From the induction law, the following can be written:

$$V_P = N_P \frac{d\phi}{dt} = N_P \cdot A_e \frac{dB}{dt} \tag{9-5a}$$

$$V_P = L_M \frac{di_M}{dt} \tag{9-5b}$$

where : B is the flux density [T], and

A_e is the effective core area [m^2].

From Eq's (9-5a) and (9-5b):

$$L_M = N_P . A_e \frac{dB}{di_M} \tag{9-6}$$

But generally :

$$B = \mu \cdot H = \mu \frac{N_P \cdot i_M}{l_e} \tag{9-7}$$

Therefore,

$$\frac{dB}{di_M} = \frac{\mu \cdot N_p}{l_e} \tag{9-8}$$

Eq's (9-6) and (9-8) give:

$$L_M = N_P A_e \frac{\mu N_P}{l_e} = N_P{}^2 \frac{A_e}{l_e} \mu = A_n N_P{}^2 \tag{9-9}$$

where $A_n = \frac{A_e}{l_e} \cdot \mu$ is the core factor.

Eq. (9-9) shows that to increase L_M, a core with higher permeability, μ, is required, with a large effective area, A_e, and a small effective magnetic path, l_e. Also, L_M can be increased by increasing the number of primary turns which has a considerable effect on the magnetising current since L_M is proportional to $N_P{}^2$. However, increasing N_P reduces the flux density, B [see Eq. (9-5a)]. This in turn, reduces the power that the transformer can transfer. It is worth mentioning here that the power available to transfer by transformers is proportional to the rate of change of the flux density as follows [4]:

$$P = f_{SW} \cdot V_e \int_{B_L}^{B_H} H dB \tag{9-10}$$

where: f_{SW} is the switching frequency [Hz],

V_e is the effective core volume and equals $A_e \cdot l_e$ [m^3], and

B_L and B_H are the minimum and maximum working flux densities, respectively.

Therefore, the number of turns is limited by the power requirements rather than the magnetising current.

9-4 EQUIVALENT SERIES RESISTANCE (ESR)

9-4-1 Introduction

One of the important applications of capacitors is in filters in power supplies to reduce the output ripple voltage. Two ripple components exist at the same time. The first component is due to the capacitor value itself, where the voltage drop across it is given by:

$$\Delta V_C = \frac{1}{C}\int_{t_1}^{t_2} i\,dt \qquad (9\text{-}11)$$

where t_1 and t_2 are the beginning and the end of the "on" time [sec],

i is the ripple current in the capacitor [A], and

C is the capacitance [F].

During the time (t_2-t_1), the ripple current i defined by the filter inductance, ramps in the capacitor. The component, ΔV_C, is in quadrature with the ripple current and is not sinusoidal. The second component is due to the resistive component of the capacitor, and it is triangle in form and in phase with the ripple current. The total ripple voltage of the capacitor is the vectorial sum of the above two components.

The resistive component of a capacitor is the sum of many physical aspects of the capacitor, and is called the Equivalent Series Resistance, or *ESR*. The *ESR* can be given by:

$$ESR = DF / 2\pi fC \qquad (9\text{-}12)$$

where f is the operating frequency [Hz],

DF is the dissipation factor or power factor, PF.

DF varies with f, C, the dielectric resistance, R, and any other condition, e.g., temperature or moisture, which causes C or R to change. Hence, when DF is used to determine ESR, it should be made at the frequency at which the capacitor is to operate. ESR and DF increase significantly with frequency due to the increase in the dielectric resistance to changes in polarization and more importantly the increase in resistance of the metal oxides at each of the interfaces. In wet electrolytic capacitors, ESR increases as they age, i.e. the electrolyte paste dries out.

9-4-2 Effect of the ESR

If the capacitor is used in the output filter in a switching power converter, then the magnitude of the ripple voltage due to ESR can be given by:

$$\Delta V_{ESR} = i \cdot ESR \tag{9-13}$$

where i is the ripple current flowing in the capacitor.

This voltage is significantly larger than the ripple caused by the capacitor value, ΔV_C.

On the other hand, the ESR of the filter capacitor plays an important role in the stability of the switching power supplies where, together with the capacitance, introduces a zero in the transfer function of the closed loop of the system. This zero should be taken into consideration when designing the compensation network of the error amplifier in the feedback loop to satisfy the criteria for a stable loop.

Hence, ESR is a critical parameter to the performance of switching power supplies, and should be reduced as much as possible, and accurately measured. It is useful to emphasize here that reducing the ESR, by choosing a good quality capacitor, is much better than increasing the value of the capacitor itself.

9-4-3 *ESR* Measurement

Fig. 9-6a shows the equivalent circuit of an electrolytic or tantalum capacitor, while Fig. 9-6b shows a circuit used to measure its *ESR*. Fig. 9-6c shows the pulse waveform of the input and output voltages of the circuit in Fig. 9-6b. L_S is only important at very high frequencies.

From Fig. 9-6b, if the external resistor R is much larger than ESR , the current i is given by: $i = V_{IN} / R$. Therefore, ESR can be found from:

$$V_{ESR} = i \cdot ESR = \frac{V_{IN}}{R} \cdot ESR \Rightarrow ESR = \frac{V_{ESR} \cdot R}{V_{IN}} \qquad (9\text{-}14)$$

from which the ESR can be evaluated, where V_{ESR} is measured by a CRT, and V_{IN} and R are pre-determined. For large capacitors which have lower ESR, the current step should be quite large to get a measurable V_{ESR}.

The circuit shown in Fig. 9-7 was built based on the above theory to measure the ESR of capacitors. The capacitor used for this purpose has a typical capacitance of 4700 μF type EG from Roederstein and has a CR (capacitance times ESR) product of $190 \cdot 10^{-6}$@ 100 Hz [5] [see App. (9)]. According to [5], ESR is calculated as follows:

$$ESR = \frac{190 \cdot 10^{-6}}{4700 \cdot 10^{-6}} = 40.4 \text{ m}\Omega \qquad (9\text{-}15)$$

Using the circuit shown in Fig. 9-7, V_{ESR} was measured to be 36.5 mV @ 100 Hz. The current was calculated from the voltage drop across R_2 to be 1.02 A when Q_1 is "off". Hence:

$$ESR = \frac{36.5mV}{1.02A} \approx 35.7 \text{ m}\Omega \qquad (9\text{-}16)$$

The capacitor value was measured by an LCR meter and found to be 5860 μF @ 100 Hz instead of 4700 μF. In this case, according to the data sheet, ESR is calculated as:

$$ESR = \frac{190 \cdot 10^{-6}}{5860 \cdot 10^{-6}} = 32.4 \text{ m}\Omega$$

This value is very close to the calculated one of 35.7 mΩ. Another sample was taken from another type of capacitors, and the *ESR* was found to be in a close approximation to that given in the data sheet.

In the circuit shown in Fig. 9-7, R_2 should be non-inductive resistor. C_3 is used to eliminate the oscillation generated due to the inductance of the long wires from the power supply to the board, and is connected directly at the entrance of power supply leads. The length of the wires along the path: C_3, R_2, C_2 and ground, should be as short as possible to reduce any stray inductance. The circuit provides a facility through a variable resistor, R_1, to change the frequency at which the *ESR* of the capacitor is supposed to be measured. This circuit was packaged in a suitable metal box and used in the lab for future *ESR* measurements.

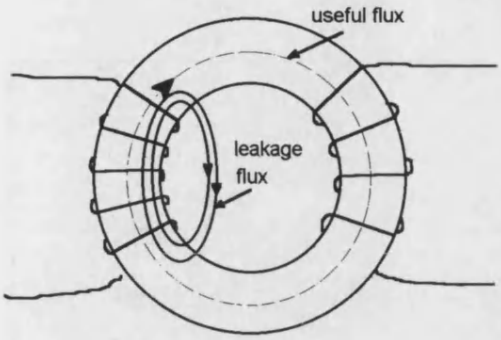

Fig. 9-1 Leakage and useful flux in transformers

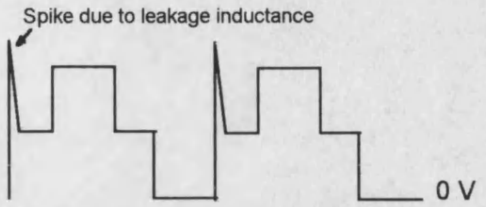

Fig. 9-2 Collector voltage in push-pull converters

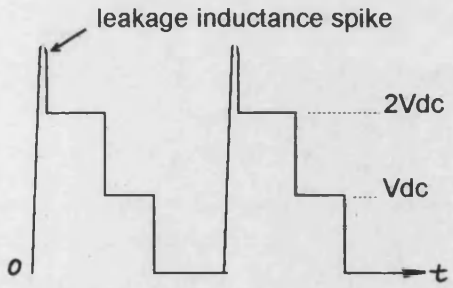

Fig. 9-3 Collector voltage in forward converters

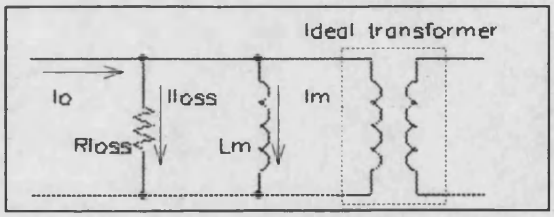

Fig. 9-4 Equivalent circuit of a transformer including L_M and R_{LOSS}

Fig. 9-5 Permeability versus flux density for 3C85 grade @100 °C

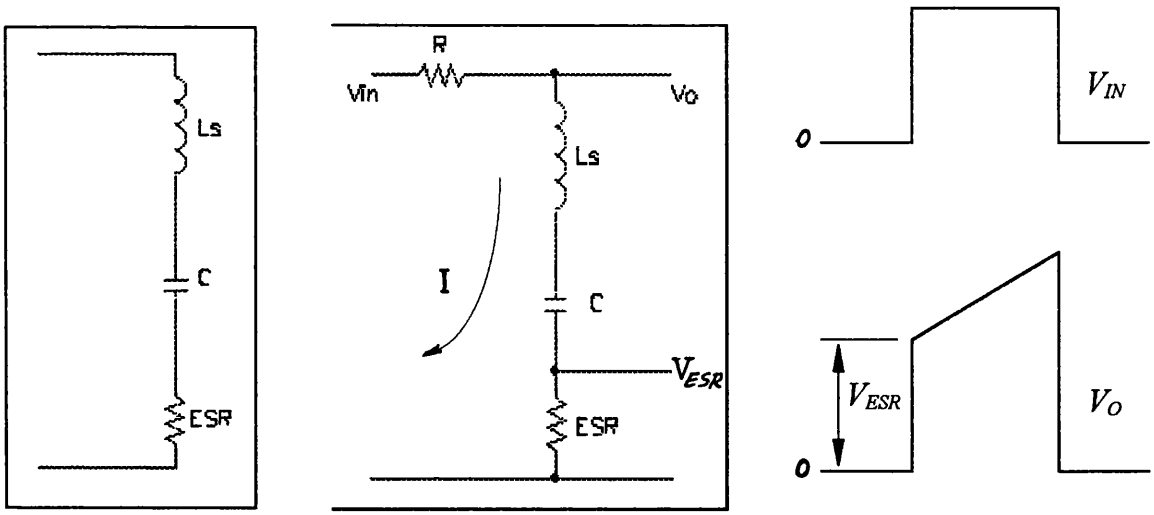

Fig. 9-6 a) Equivalent circuit of a capacitor, b) a circuit to measure the *ESR*, and c) input and output voltage waveforms

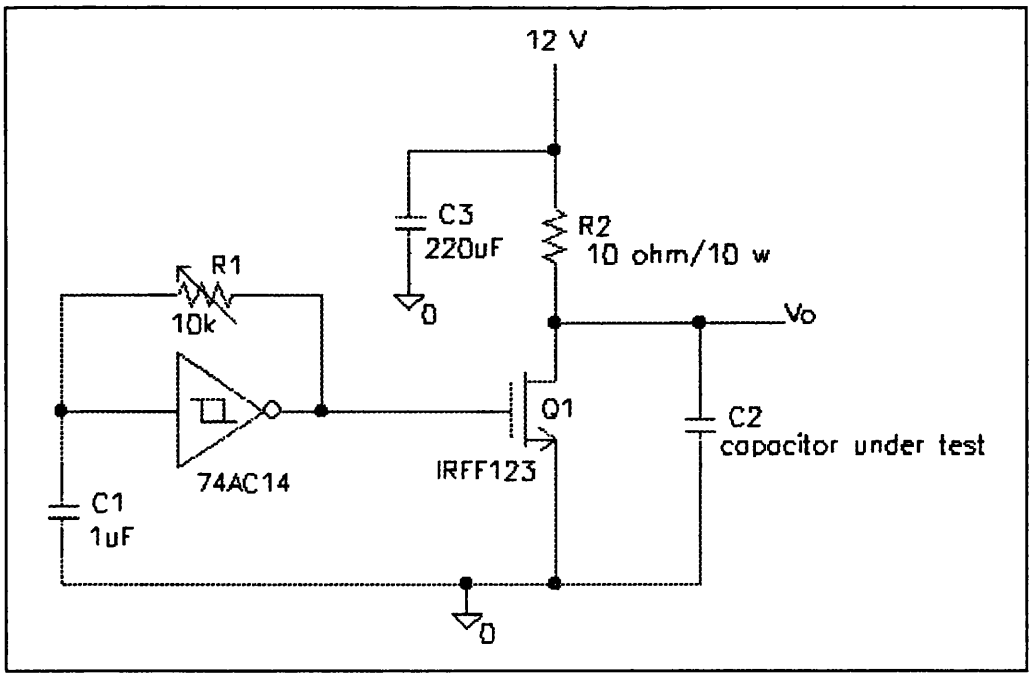

Fig. 9-7 A circuit for measuring *ESR* of a capacitor

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PSPICE VERSUS MATLAB

10-1 INTRODUCTION

The PSPICE circuit simulator enables the user to quickly create, simulate, and test circuit designs which contain analogue and digital components, through its schematic entry capability, or through creating a netlist description of the circuit to be simulated [1, 2, 3]. Therefore, in order to simulate a circuit, there is no need to completely understand the function of each component in the simulated circuit, or to write the differential equations that describe the behaviour of the circuit. In contrast, MATLAB is a numerical simulator and is not designed for circuit simulation. Therefore, the user must create the mathematical component models and set up systems of differential equations to simulate a circuit. In some cases, e.g. where typical waveforms are required for examination, it is beneficial to use MATLAB in order to avoid intrinsic problems that exist in PSPICE, though this is not always an easy task. The next sections describe PSPICE problems and how they can be avoided.

10-2 PSPICE PROBLEMS

10-2-1 Long Computation Time

The main problem when using PSPICE to simulate high frequency circuits is the time required by the program to finish simulating the time range of interest which may include several thousand high-frequency cycles.

During analogue analysis, PSPICE maintains an internal time step which is continuously adjusted to maintain accuracy while not performing unnecessary steps. During non-active periods of circuit operation, the time step is increased, and during the active periods, it is decreased [1]. If the circuit has very high frequency signals , and high accuracy is required, the time step is adjusted to suit these requirements. This results in very short time steps and, hence, very long computation time.

This problem becomes a particular nuisance when long time constants, i.e. low natural frequency signals, exist in the simulated circuit which also contains high frequency signals. If it is required to examine these low frequency signals, the *Final Time* parameter, which is the real simulated time will be long. Also PSPICE will reduce the time step in order to follow the high frequency signals and to stay below the required tolerance. This results in a very long computation time which, in some cases, can take several days!

10-2-2 Non-Convergence Problems

In order to simulate electrical circuits, PSPICE solves a set of non-linear equations that describe the behaviour of the circuit. This is done using Newton-Raphson algorithm [4, 5], which is an iterative technique. In some cases, PSPICE cannot find a solution to these equations, and the simulation comes to a halt with a non-convergence error message. Examining the output file of the simulated circuit can help in detecting the reason for the error, e.g. if a very high current or voltage spike is generated.

10-2-3 Large Required Memory for Data Files

The results of the simulated circuit are saved in a file called "*filename*.dat", which is used by *Probe* to visualise different waveforms. This data file is very large and takes quite a large size of memory space. This not only has the effect of increasing the memory size required, but also slows down visualising the required waveforms in *Probe*.

The following section describes some experience gained in overcoming PSPICE simulation difficulties. If these ideas fail to solve the difficulties satisfactorily, MATLAB or some other program may have to be used to generate typical circuit waveforms.

10-3 SOLVING PSPICE PROBLEMS

10-3-1 Reducing Computation Time

10-3-1-1 Initial conditions

Initial conditions can be voltages across capacitors, or currents in inductors. Initial conditions of magnetic flux density, B, in transformers, on the other hand, is not available at the time of this writing. To solve initial condition problems in transformers, refer to Ch. 12.

Applying initial conditions allows the circuit to reach the steady-state quickly, thus reducing the *Final Time* required to simulate the circuit. Setting initial conditions may also help in avoiding non-convergence problems, since PSPICE is told to start from pre-defined values rather than trying to find a solution for the first time step.

10-3-1-2 Using Save and Load Bias Point

Saving and restoring bias point calculations can significantly decrease simulation times when large circuits are run multiple times, and can aid convergence [1].

10-3-1-3 Number of simulated cycles

Reducing the number of simulated cycles, reduces the total simulation time. If initial conditions are properly set, two or three cycles may some times be enough.

If initial conditions are not known, large number of cycles are required. In this case, it is possible to obtain non-convergence problems. To help solve this, the number of simulated cycles may be reduced, and voltage and current values at the end of the simulation can be used as initial conditions for the next simulation. This can be repeated if steady-state condition is not reached.

10-3-1-4 Effect of RELTOL

The accuracy of PSPICE analogue results is controlled by the parameters *RELTOL*, *VNTOL*, *ABSTOL*, and *CHGTOL*. The most important of these is *RELTOL*, the relative tolerance, which controls the relative accuracy of all voltages and currents which are calculated [1]. The default value of *RELTOL* is 0.001. If higher accuracy is needed, this figure can be decreased to 0.0001 or even lower. If lower accuracy is tolerated, *RELTOL* may be increased to 0.01 or, for rough and fast simulation, to 0.05.

Increasing *RELTOL* has a considerable effect on reducing the simulation time, as PSPICE is allowed to increase the time step in this case.

For example, a forward converter as shown in Fig. 10-1 was simulated with set-up parameters as follows:

ABSTOL: 100 μA, *CHGTOL*: 0.01 pC, *RELTOL*: 0.002, *VNTOL*: 100 μV,

Print Step: 100 ns, *Final Time*: 20 μs, *Step Ceiling*: 50 ns,

Initial conditions: Inductor current: 2 A, Capacitor voltage: 4.8 V.

The computation time on 25 MHz computer was 223 s. By increasing *RELTOL* to 0.02 instead of 0.002, the computation time was decreased to 128 s, which shows that computation time is related to *RELTOL*.

Note:

Some times a ripple can be seen in some waveforms, such as diode currents in forward converters. This ripple, if it is not a real ripple, may be due to numerical instability resulting from increasing *RELTOL* too much. This ripple does not appear in the forward converter inductor current, which may be due different algorithm used to

solve these currents. If this occurs, *RELTOL* should be decreased to an acceptable level.

10-3-1-5 Eliminating high frequency oscillation

High frequency oscillations usually exist in switch-mode power supplies due to resonance between stray wiring inductance and the parasitic capacitance of semiconductors. These oscillations increase simulation time to very high values because PSPICE reduces the time step to very small values to follow all the changes in currents, voltages and charges. To speed up simulation, this oscillation should be minimised or even eliminated. A straight forward remedy for this problem is to use proper *RC* snubbers across power diodes and switches.

10-3-1-6 Reducing switching speed

If semiconductor switches or even ideal switches are used in the circuit, it is preferable to close and open them at reasonable speed, since fast switching speed generally creates high current and voltage transients especially if series inductance or parallel capacitance is broken or short-circuited rapidly. This can help increasing the rise and fall times of signals, thus allowing an increase in the *Step Ceiling* parameter without non-convergence problems. Increasing the *Step Ceiling* allows PSPICE to increase the time step and, hence, increase the simulation speed.

For example, a zero-voltage-switching full-bridge converter (zvs-fb) as shown in Fig. 10-2 was simulated and took 3.5 hours. It was not possible to increase the *Step Ceiling* further, until the range of *E*-table was reduced, which means reducing the switching speed. As a result, *Step Ceiling* was increased to 5 ns instead of 2 ns, and the simulation took about 1.13 hour (compared with 3.5 hours).

Reducing the rate of change of voltages and currents as a result of reducing switching speed, not only allows higher *Step Ceiling* to be used, but also increases the time step during transitions, which further increases the speed.

10-3-1-7 Increasing Step Ceiling

Step Ceiling is the maximum time step allowed for PSPICE. It is set to prevent PSPICE from increasing the time step to allow signals with high frequency content to be examined. If short duration signals need not be examined, then increasing this parameter reduces the simulation time. Therefore, it is possible to increase it as much as possible, provided it stays below the periods of interest.

Some times, increasing *Step Ceiling* might cause non-convergence problems. In this case, it should be decreased, and other solutions for reducing simulation time should be used.

10-3-1-8 Reducing the number of components

Computation time increases as the number of components in the simulated circuit increases. Therefore, the number of components should be minimised wherever possible. One example of doing this is by using a current source in the output of a power supply instead of using an *LC* filter and a load resistor.

Fig. 10-3a shows a push-pull inverter with the components used to include a dead time between the "on" pulses. The simulation time was 24.2 min on a 25 MHz computer. Later these components were eliminated from the circuit, as shown in Fig. 10-3b, and the dead time was included in *E*-tables, E_1 and E_2. The simulation time in this case was 10.4 min, i.e. a reduction of 57% is achieved.

10-3-1-9 Using analogue behavioural modelling

Analogue behavioural models can be used to replace complicated circuits or IC's. This has the effect of reducing the simulation time. On the other hand, it is not recommended to use them to replace simple circuits as it takes more time than required using the original circuit.

10-3-1-10 Using ideal components

Integrated circuits are simulated in PSPICE by sub-circuits. The number of the sub-circuits which are used to resemble the integrated circuit, and therefore the number of components used, depends on the complexity of the circuit. If, however, typical waveforms are to be examined, integrated circuits can be substituted by ideal

components. This makes it easy for PSPICE to analyse the circuit, and, therefore, reduce the simulation time. This also helps in avoiding non-convergence problems which may result from the original integrated circuit.

Examples of this are to use ideal switches instead of transistors, *E*- or *G*-tables instead of comparators, V-pulse voltage sources instead of function generators, etc.

However, using ideal components, such as switches, may some times cause non-convergence problems if the simulated circuit has, for example, a current or a voltage that is switched rapidly. In this case, some parasitic components should be added to reduce the switching speed.

10-3-1-11 Working in parallel with PSPICE

When running PSPICE, the output results (to be distinguished from the data) are written to a file called "*filename*.out". In this file, the time taken by PSPICE to do the job is included. This time is the total time taken including the time during simulation when the user is doing some other job, such as examining waveforms, printing, etc. All this time is recorded as simulation time, though it is not all spent on simulation. For example, one circuit has taken 121 s as a pure simulation time when no other job was done during simulation. This time was increased to 360 s when different waveforms were examined during circuit simulation.

10-3-2 Solving Non-Convergence Problems [1, 6]

10-3-2-1 Increase iteration limits, *ITL1* and *ITL4*.

10-3-2-2 Increase *RELTOL*.

10-3-2-3 Increase *ABSTOL*, *CHGTOL* and *VNTOL*.

10-3-2-4 Decrease *Step Ceiling* and *Final Time*.

10-3-2-5 Use snubbers across fast switching devices to reduce the rise and fall time, especially across rectifiers, freewheeling diodes and power switches.

10-3-2-6 Use high resistors across inductors, particularly if there is capacitances which can cause resonance.

10-3-2-7 Use initial conditions if possible, as described in Sec. (10-3-1-1).

10-3-2-8 Use voltage limiters in positions where high voltages are expected.

10-3-2-9 When creating a new diode model, try to set reasonable values for *CJO* and *RS*. *CJO* = 0 can cause the diode to switch in a zero time and cause non-convergence problems [4].

10-3-2-10 Try not to push currents into very high resistances (for example, reverse-biased pn junctions). This can cause a very high voltage.

10-3-3 Reducing the Required Memory Size

10-3-3-1 Using Markers

In order to reduce the data file size, markers may be used before the simulation starts. If they are used after the simulation, no memory size is saved, but the marked points can be monitored in *Probe*.

Markers are symbols which can be placed on the schematic on selected pins, wires, or buses in order to visualise voltages, currents, and digital waveforms in PSPICE. If they are placed before simulation, they can be used to limit the results that are saved to the data file, thus reducing the memory size taken by this file [1].

10-3-3-2 Reducing number of components

If markers are not used, reducing number of components in the simulated circuit, as described in Sec. (10-3-1-8), can reduce the memory which the data file needs.

10-3-3-3 Using ideal components and analogue behavioural models

Ideal components and analogue behavioural models can significantly reduce the memory size, especially if they replace very complicated circuits or components.

10-3-3-4 Increasing No-Print Delay

If the required part of the waveforms to be examined is the last part, which is usually the case, then increasing the *No-Print Delay* parameter suppresses the output of the first portion of the analysis, and allows the data of the period of interest to be saved in the data file. This, of course, reduces the memory size, and speeds up waveform processing later in *Probe*.

10-4 OTHER PSPICE PROBLEMS

PSPICE has some other problems which indicate some weakness in the PSPICE package, some of which are not interpreted. The following lists some of the main common problems encountered by the author during four years of simulation.

10-4-1 Schematic Problems

One such problem occurs if the simulated circuit is complex, and components are very close to each other. It has been noticed throughout the simulation, that wires which are not connected to each other, and not meant to be connected in the schematic, are in fact connected in the netlist. This is very difficult to detect, since it is very clear from the schematic that these wires are not connected. The only way to detect these errors is to examine the netlist of the circuit carefully, after discovering that there are some false or logically untrue signals appear when examining some waveforms.

The problem will be so dangerous if these false signals are not discovered. In this case, one may complete the simulation and draw results from this simulation without noticing that there is something wrong.

Also, even after finding the error, and trying to disconnect the wires which are incorrectly connected, it is not so easy to solve, unless deleting all components around the error point and reconnecting them again in, probably, a different arrangement.

It also has been seen that when finding these errors, another arrangement is made to solve this, and when returning to the old configuration the circuit is found to be normally working!

10-4-2 Unchangeable *Step Ceiling* During Simulation

As mentioned earlier, the *Step Ceiling* is set before the start of the simulation and is used to limit the maximum time step taken by PSPICE.

Usually, at the beginning of the simulation, the time step taken is too small, and the minimum allowed time step depends on the *Step Ceiling* and the *Final Time*, where it decreases as the *Step Ceiling* decreases.

If the required time step is less than the minimum one, PSPICE issues an error message that the time step is too small. In this case, if no change is possible in the circuit, either the *Final Time* or the *Step Ceiling* must be decreased.

The *Final Time* is usually determined by the time of interest and can not be reduced below some value. Therefore, the only parameter which may be changed in this case is the *Step Ceiling*.

Reducing the *Step Ceiling*, however, increases the computation time considerably and it is *not possible* to reduce the *Step Ceiling* at the beginning of the simulation to pass the first part of the simulation, and then increase it for the rest of the simulation in order to reduce the computation time.

To solve this problem, the same solutions to reduce the computation time may be followed as described earlier.

10-4-3 Long Display Time

When a signal is displayed in *Probe*, it takes some time for the data to be prepared and the signal be displayed. The time taken for this, increases as the data file size increases.

If now another signal is to be displayed, irrespective of being on the same axis and has the same scale or not, the previous signal will be redisplayed followed by the new signal. The time needed in this case, is the time required to prepare the data for the new signal and the time required to display both signals.

Any addition or deletion of any waveform, axis or plot, or any change in y- or x-axis scale, *Probe* will redisplay all of the remaining signal, though most of the times is not required.

Also, when printing a graph, *Probe* redisplays all of the printed waveforms when the data are prepared to be sent to the printer.

Therefore, if the data file is too big, very long time is unnecessarily required to examine or print different waveforms, which seems a weak point of the PSPICE package.

To solve this problem, it is recommended, prior to displaying any waveform, to add the required plots and axes, scale axes, and restrict the time to the range of interest. It is also preferred that all other windows, if opened, are closed to speed up *Probe* execution time.

10-5 MATLAB PROBLEMS

MATLAB requires a full understanding of the function of the circuit to be analysed. Moreover, it requires entering a set or sets of differential equations that describe the behaviour of the simulated circuit. Therefore, it is very difficult to simulate very complicated circuit, especially those involving non-linear components, such as transformers.

Editing circuits is also not an easy issue. It requires redefining functions and changing some or all of the previous equations.

On the other hand, MATLAB is quite fast compared to PSPICE, and non-convergence problems are rarely encountered. Therefore, if these problems can not be solved in PSPICE, using MATLAB to simulate electrical circuit is preferred particularly if all component models needed to simulate the circuit are available in the MATLAB library.

CHAPTER TEN REFERENCES

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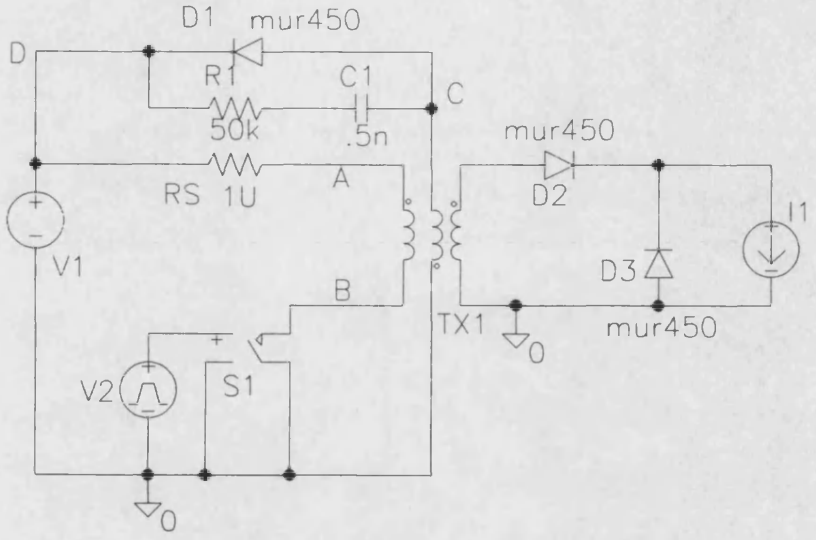


Fig. 10-1 A simulated forward converter to show the effect of *RELTOL*

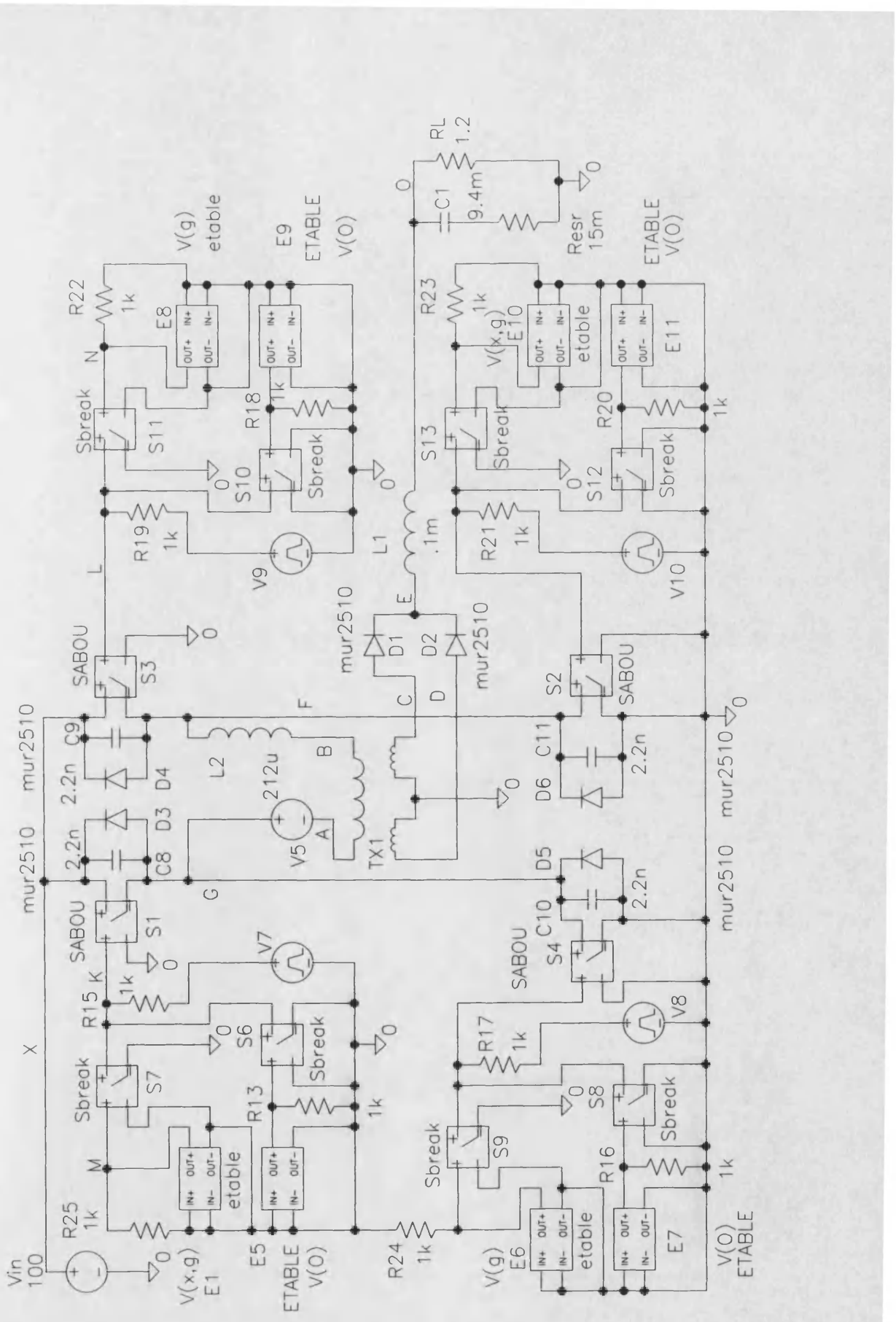


Fig. 10-2 A zero-voltage-switching converter to show the effect of the *Step Ceiling*

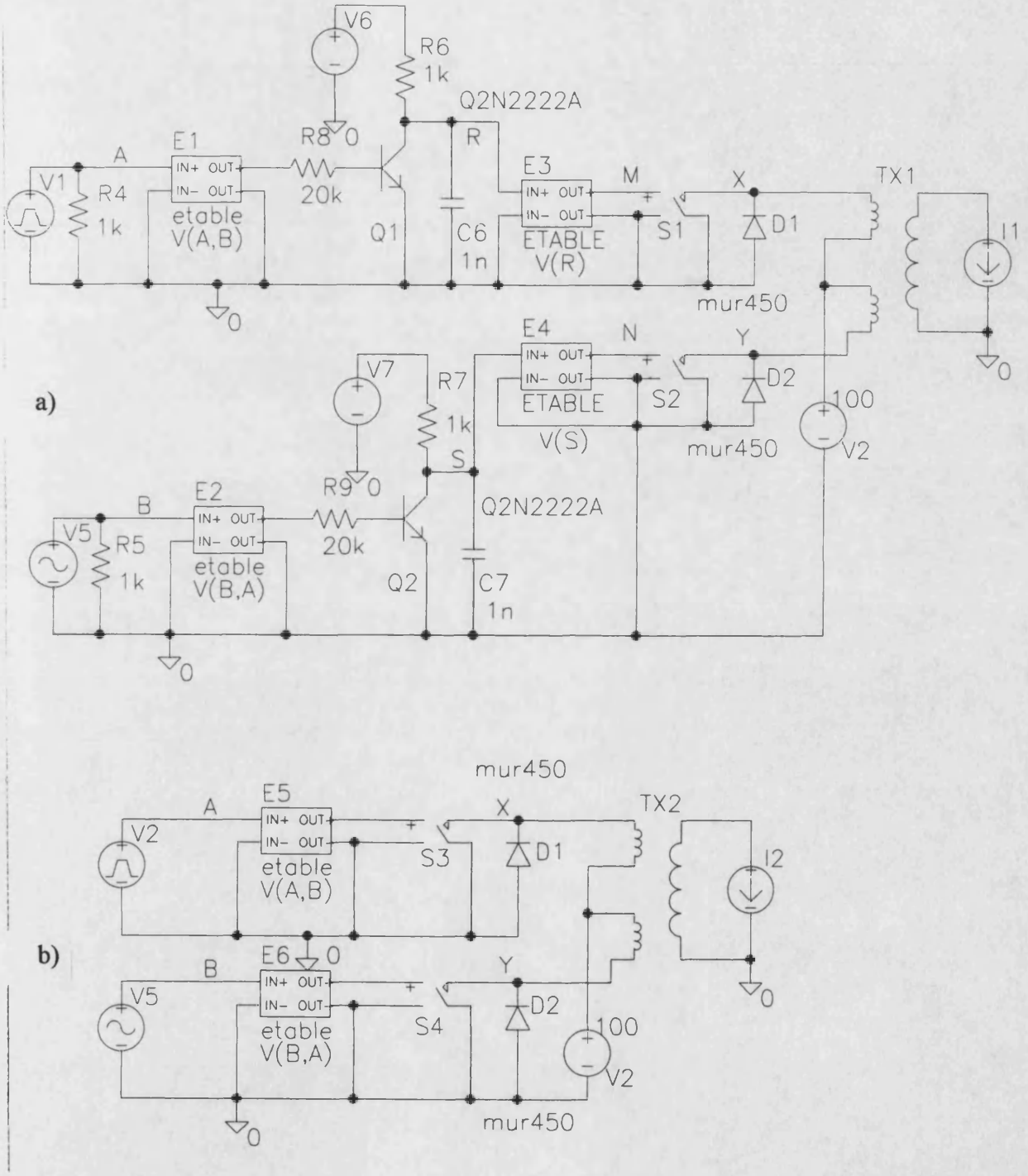


Fig. 10-3 A simulated push-pull converter to show the effect of reducing number of simulated components

MATLAB HYSTERESIS MODELING

11-1 INTRODUCTION

Power electronics circuits are modeled and simulated to gain insight into their operation, optimize their control, and optimize the use of components and materials used in them. Until recently it had been difficult to model the nonlinear behaviour of practical inductors and transformers which largely arises due to the nonlinear behaviour of the magnetic core material used. The development of a nonlinear MATLAB model is now considered.

dc/dc converter modeling has been an extensively research topic, including magnetic core modeling.

Because of the non-linearity arising from the *B/H* loops of magnetic core materials, practical inductors and transformers are very difficult to analyze via traditional analytical methods, which made it difficult to obtain an accurate model of the hysteresis phenomena.

With the continuous improvements in modern power electronics to improve wound components utilization and the design for even greater miniaturization, the study of the magnetic core behaviour becomes increasingly important. The importance of having an accurate core model increases as the switching frequency increases, since the core loss which depends on the *B/H* characteristics increases.

A non-linear magnetic core model including hysteresis and saturation, based on the Jiles-Atherton magnetic model [1] does exist in PSPICE [2-5] as mentioned earlier, and it is simple to use and quite accurate. But as presented in Ch. 10, PSPICE has its own difficulties which require using other simulators that solve some of PSPICE problems.

Attempts have been made in this report to exploit the MATLAB numerical simulator to simulate and model electrical circuits if a library containing the required element models is available.

Since this work is concentrated on isolated dc/dc converters using transformers as isolated elements, extensive work has been spent on transformer modeling in MATLAB to demonstrate the ability of such simulators to simulate electrical circuits including transformers.

The following sections illustrate how hysteresis and saturation may be modeled in MATLAB, and discuss the limitations of the model.

11-2 B/H LOOP MODEL PROCEDURE

The procedure followed to model the magnetic core *B/H* loop is briefly summarized here and is developed from [6].

The model assumes that the upper and lower branches of the hysteresis loop which form the major loop is given.

An approximate magnetization curve is calculated from the average of the upper and lower branches of the major loop, and is defined when H and B start from zero and increase or decrease without reversal. The magnetization curve can, therefore, be calculated as follows:

$$B_{MAG}(H) = \frac{B_L(H) + B_U(H)}{2} \qquad (11\text{-}1)$$

where $B_{MAG}(H)$ is the flux density as a function of the field strength for the magnetization curve,

$B_U(H)$ is the flux density of the upper branch of the *B/H* loop, and

$B_L(H)$ is the flux density of the lower branch of the *B/H* loop.

The minor loops are the curves followed if H is varied within $-H_{MAX}$ to $+H_{MAX}$ cyclically.

The upper branch of the minor loop is approximated by shifting the upper branch of the major loop downwards by an amount B_d where $0 \leq B_d \leq B_r$, as shown in Fig. 11-1. The lower branch of the minor loop is approximated by shifting the lower branch of the major loop upwards by the same amount B_d.

11-3 OBTAINING THE MAJOR LOOP

Minor loops are approximated from the major loop which is assumed to be given. The major loop of any core material can be obtained either from the data sheet of the required ferromagnetic material or through measurements. Alternatively, as accomplished in this report, the major loop can be obtained from PSPICE which is based on the Jiles-Atherton magnetic core model.

The material chosen for this purpose is 3C8, where the magnetic flux density, B, of the upper and lower branches of the hysteresis loop as a function of the magnetic field strength, H, are given in App. (11). App. (11) shows only the positive values of H, and the corresponding $B_U(H)$ and $B_L(H)$. For negative H values, the upper and lower B values are interchanged after changing their sign. All H values used in this chapter are in Oersted [Oe] as that used in PSPICE.

11-4 HYSTERESIS MODELING USING LOOK-UP TABLES

Fig. 11-2 shows how the major and minor loops may be obtained following the procedure given in [6]. The model uses look-up tables "B_L" and "B_U" in which lower and upper branch values as a function of H are stored. S_1 is used to switch

between the two curves depending on dH/dt. B_{dL} is the difference between the current B value and the lower branch of the major loop, while B_{dU} is the difference between the current B value and the upper branch of the major loop. This value, which is B_d in Fig. 11-1, should be subtracted from the corresponding curve when dH/dt reverses direction. B_{MAG} represents the magnetization curve values which is calculated according to Eq. (11-1) where k = 0.5. The "t" clock and the constants 111 and -111 are employed to give the magnetization curve values. The blocks F_6, F_7 and S_7, S_8 are used to force the B values to follow the magnetization curve when required. S_9, S_{10} and S_{11} are used to solve the problem of the step which the curve takes when it reverses direction in order to follow the magnetization curve, when it is not required. Blocks S_9 and S_{10} use the sign of B to decide whether to jump to the magnetization curve or not.

Fig. 11-3 shows some minor loops obtained from the model of Fig. 11-2. It can be seen that the model fails at small values of B and H. Also, it can be seen that the curves are not smooth due to using look-up table values.

11-5 HYSTERESIS MODELING USING CURVE-FITTING TECHNIQUE

To improve the model of Fig. 11-2, curve fitting technique is used instead of look-up tables in order to calculate the B values. App. (11) is used in EasyPlot software to obtain the equations that match the two parts of the major loop when H is positive. When H is negative, the same two curves are used to extract B values as described in Sec. (11-3). Fig. 11-4 shows how the major loop can be obtained using curve fitting technique. The equations found to acceptably fit the lower and upper branches of the hysteresis loop of the 3C8 ferrite material grade for positive H values are as follows:

$$B(H) = a + be^{-H/c} + dH^f e^{-H/g} \qquad (11\text{-}2)$$

where for the lower branch :

$a = 384.6$, $b = -498.4$, $c = 0.7418$, $d = 27.7$, $f = 0.8152$ and $g = 20.31$,

and for the upper branch:

$a = 318.6$, $b = -207.7$, $c = 0.6878$, $d = 86.86$, $f = 0.4202$ and $g = 40.04$.

Fig. 11-5a shows the lower branch resulted from using Eq. (11-2) with the first set of data, while Fig. 11-5b shows the upper branch resulted from using the same equation with the second set of data. Also shown on each graph are the data given in App. (11) which show a good agreement between Eq. (11-2) and App. (11). Fig. 11-5c shows the major and minor loops resulting from Eq. (11-2) and Fig. 11-4 (compare with Fig. 11-3). Fig. 11-5d shows the major loop at very high H values, while Fig. 11-6 shows the complete B/H loop model using curve-fitting technique.

11-6 USING SEPARATE EQUATION FOR EACH BRANCH

As shown in Fig. 11-5c, at values of H around zero, the curve has a step change because it changes the equation; the equation used for the positive H values is not the same as that used for the negative H values. This step in the curve causes B to change abruptly at zero H values. To solve this problem and improve the appearance of the loops, only one equation for each part of the hysteresis loop should be used; one for the whole upper branch and one for the whole lower branch. Using complete values for H (negative and positive), the following equation was found to fit the major loop very well:

$$B = a \arctan[b(H - c)] \qquad (11\text{-}3)$$

where for the lower branch:

for $H \geq 5$ Oe: $a = 319.6$, $b = 1.666$, $c = -0.2152$

for $H < 5$ Oe: $a = 5.578$, $b = 1.666$, $c = -0.2152$

and for the upper branch:

for $H \geq 5$ Oe: $a = 319.6$, $b = 1.666$, $c = 0.2152$

for $H < 5$ Oe: $a = 5.578$, $b = 1.666$, $c = 0.2152$

Fig. 11-7a, b and c shows the curves for 3C8 material grade as obtained from Fig. 11-6, and data as obtained from PSPICE which shows a very good agreement between the actual B values and the calculated ones.

11-7 CONCLUSION

When trying to model a transformer using Fig. 11-7c, it is found that it is difficult to obtain μ (= dB/dH). The reason for this is that when H changes direction at the far end of both sides of the hysteresis loop, the equation used to calculate B changes. Although this is not seen in Fig. 11-7c because the error is very small, but because of the inevitable error between the calculated values and the actual data, the values of B calculated at $-H_{MAX}$ and $+H_{MAX}$ are different for each equation. This in turn causes a step in B values at the ends of the hysteresis loop which causes μ to have very high values and causes oscillation in the closed loop of the transformer model.

Another limitation of the model stems from the fact that the procedure itself does not inherently seem to work well at very small minor loops, and/or for converters that use only one half of the hysteresis loop such as forward and flyback converters, although this is not mentioned in [6].

Therefore, alternative MATLAB transformer modeling techniques will be investigated as will be described in the next chapter.

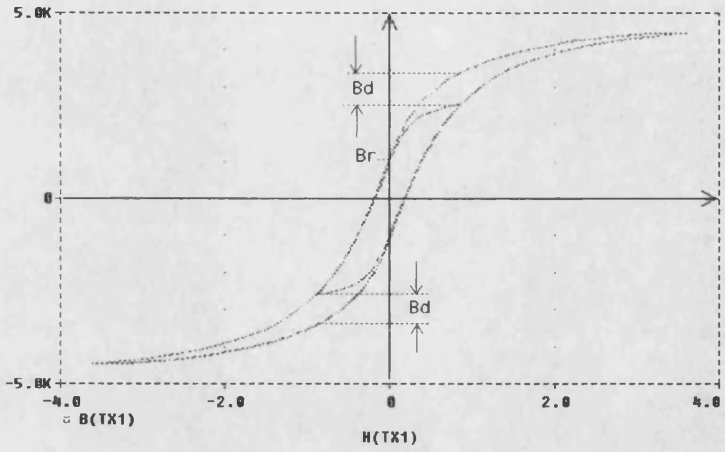


Fig. 11-1 Obtaining minor loops from the major loop

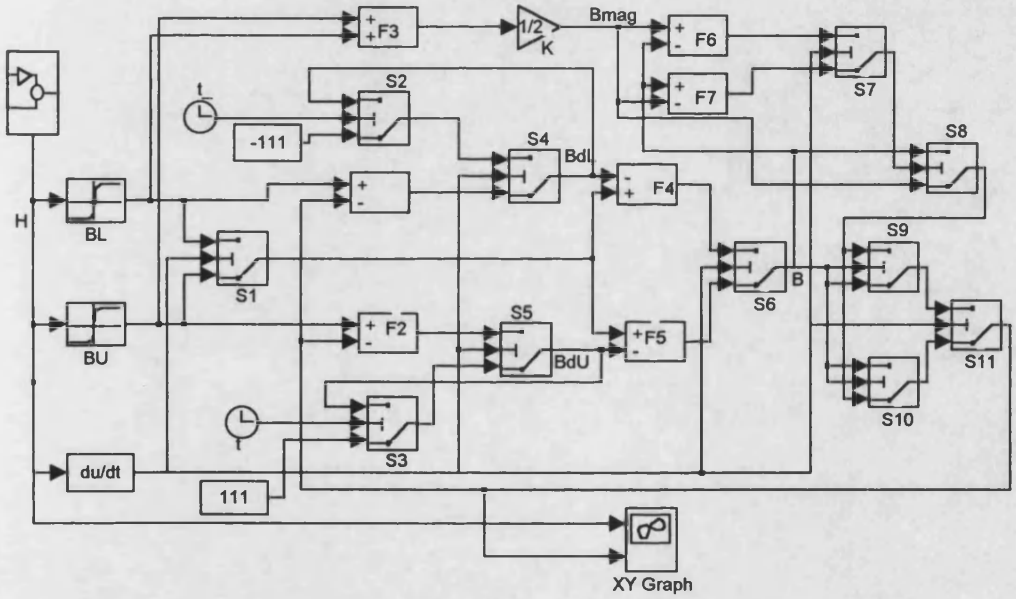


Fig. 11-2 Modeling *B*/*H* loop in MATLAB using look-up tables

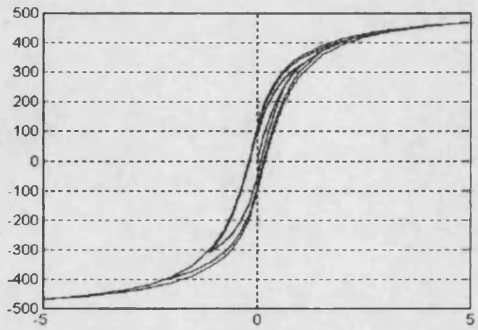


Fig. 11-3 Minor loops for 3C8 ferrite material grade as obtained from Fig. 11-2

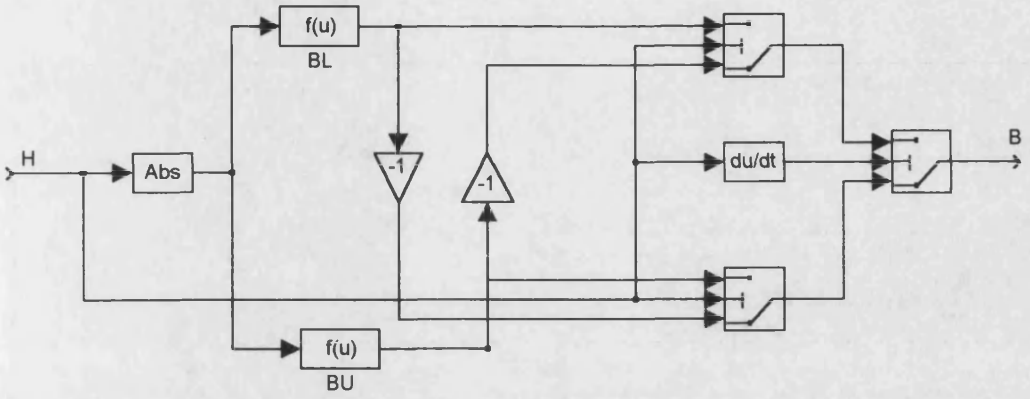
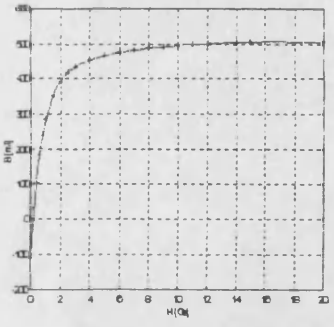
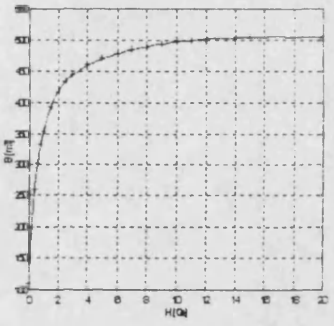


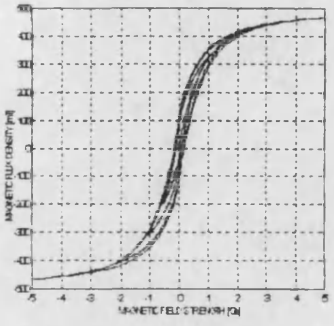
Fig. 11-4 Extracting the major loop using curve-fitting technique



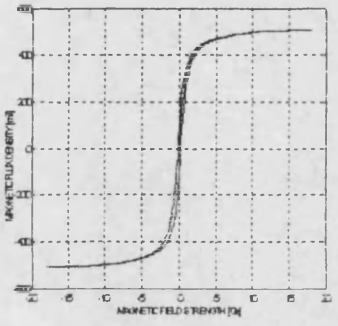
(a)



(b)



(c)



(d)

Fig. 11-5 a) The lower branch and b) the upper branch as obtained from Eq. (11-2), c) the major and some minor loops obtained from the model shown in Fig. 11-6, and d) the major loop at high H values

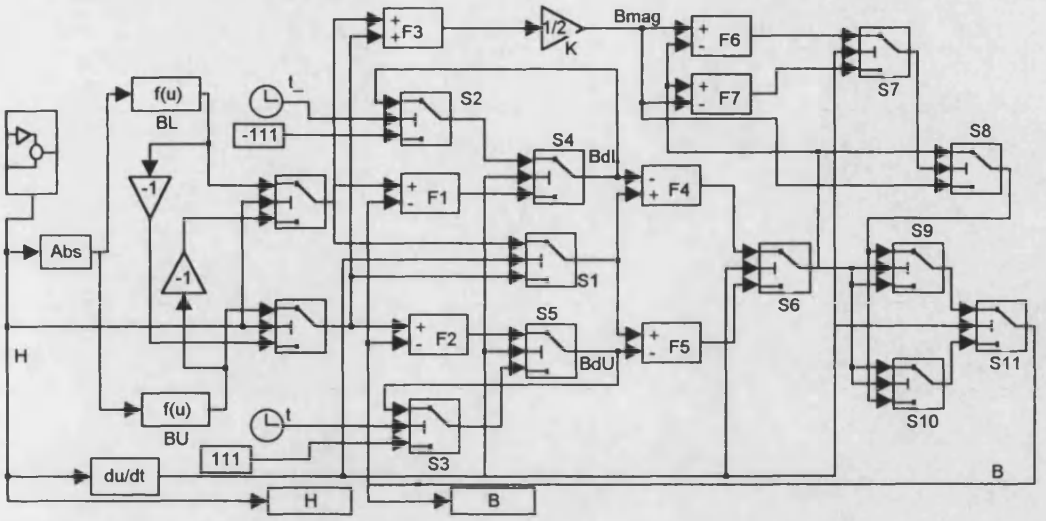
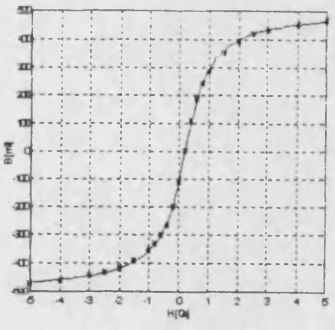
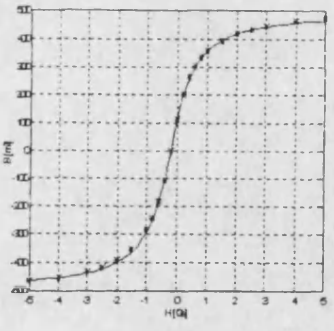


Fig. 11-6 The complete *B*/*H* hysteresis loop model using curve-fitting technique



(a)



(b)

c)

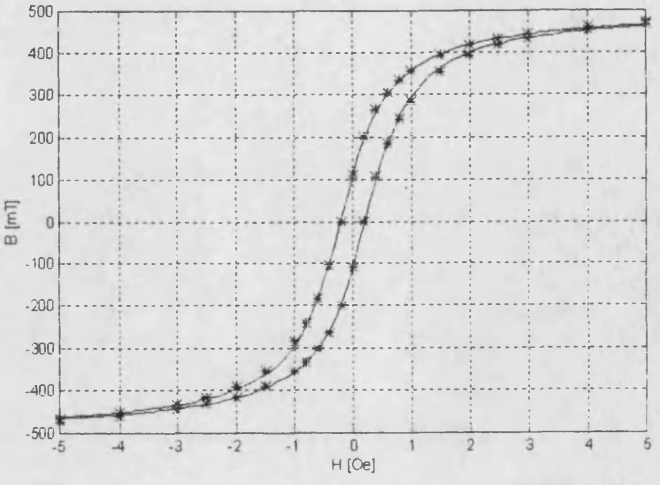


Fig. 11-7 a) The lower branch, b) the upper branch and c) the major hysteresis loop as obtained from Eq. (11-3)

CHAPTER ELEVEN REFERENCES

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SINGLE-PHASE TRANSFORMER MODELLING

12-1 INTRODUCTION

Practical transformers are quite difficult devices to model because of their non-linear, temperature-dependant electromagnetic behaviour.

In the PSPICE circuit simulator, a method of simply modelling a non-linear single-phase transformer exists and is quite well developed. Both magnetic hysteresis and saturation behaviour may be relatively accurately modelled for a range of core-material types. The *B/H*-loop data for any new, or previously unspecified, core-type may be approximated and added to a library of core types. Non-linear PSPICE inductor and transformer models may then be readily constructed using this and allow the steady-state operation of power-electronic circuits to be relatively simply and faithfully simulated.

One limitation of the model is that the user is not able to easily set initial conditions for the magnetic flux-density, B, in the core. Therefore, the user is not able to adjust initial core conditions to reflect worst-case practical initial conditions which may cause high transient currents in the transformer primary.

Non-linear three-phase transformers are also not readily modelled in PSPICE using simple components and default settings, and a careful study has been conducted to develop an acceptable model. The resultant model has been tested theoretically and compared with published results, and found to give acceptable results.

While the PSPICE circuit simulator with its schematic entry capability allows circuit simulations to be quickly set up and edited later, second-order component effects,

particularly in semiconductor device models, frequently cause unnecessarily high-resolution time stepping, thus slowing down the simulation of switched power-electronic circuits and post-processing of results considerably, and creating the need for significantly higher memory to store all the data produced. Using a numerical simulator, such as MATLAB, and a more idealised functional description of circuit operation, often allows typical waveforms and salient performance indicators to be computed over a range of operating conditions, say for system optimisation, much more rapidly than with a circuit simulator such as PSPICE. However, to date, a non-linear transformer model for MATLAB with similar capabilities as the PSPICE model does not appear to have been developed. A literature survey on transformer modelling in MATLAB have been conducted covering the period 1982-1996 to check for any existing models. Considerable time has, therefore, been spent developing a single-phase MATLAB transformer-model to improve the ways and speed of simulating transformer-isolated switching power-converters.

12-2 PSPICE NON-LINEAR SINGLE-PHASE TRANSFORMER MODEL

PSPICE, as previously noted, provides a good non-linear single-phase transformer model, except that there is no possibility of setting initial conditions for the flux and field strength in the model.

It is well known that the flux, ϕ, in any raw non-magnetised core starts from zero, and increases in one of two possible directions depending on the polarity of an applied winding voltage. As the field strength is increased, the initial variation in flux is governed by the core material magnetising curve, as shown in Fig. 12-1.

When a voltage, v_P, is applied to a winding of N turns on a core, the flux at any time is given by:

$$\phi = -\frac{1}{N}\int_0^t v_P \, dt + C \qquad (12\text{-}1)$$

In most practical situations, the constant of the integration is not zero because of the residual core flux density, i.e. the remanance. In the PSPICE model, however, it is always assumed that virgin core material is used to start with. Hence, the constant of integration is always taken to be zero at the start of the simulation.

If a sinewave voltage is applied to the winding, under steady-state conditions the flux will have the same waveshape and also be sinusoidal with a 90° phase shift as shown in Fig. 12-2. Also, it should be centred around zero as the applied voltage is. This means that when the voltage is at a peak value the flux is zero, and when the voltage is zero the flux is at a peak value. Therefore, if the voltage starts from zero, the flux should have a value of - ϕ_{max} and not the zero value initially shown in a PSPICE transformer model with initial virgin core material.

In the PSPICE model, if the voltage started from zero, the resulting variation in flux will be similar to that shown in Fig. 12-3, where the increase in flux from zero starts when the voltage is zero. The increase continues for as long as the voltage is positive (because of the integration), and reaches a peak when the voltage changes polarity. From the flux waveform, it can be seen that it is not centred around zero as it should be, and the core may saturate if it is normally operated close to saturation, as is often the case in practical applications.

Saturation may be detrimental in practice, e.g. causes power semiconductor device failure or nuisance fuse tripping, if the voltage source resistance and the transformer primary circuit resistance are very low, because it will persist for a relatively long time. The exact time is set by the magnetising inductance and primary-circuit-resistance time-constant [1, 2, 3]. As primary circuit loss increases due to copper and core heating, the transient flux decreases to its normal zero value more rapidly and the core flux begins to cycle around zero [1], i.e. a steady-state core flux waveform is reached. Another way of looking at this is that the high core flux is produced by a high magnetising current. This flows in R_S, the primary circuit resistance, and reduces the transformer primary voltage. Hence, the flux will not be able to maintain its peak value, and will rapidly tends towards symmetry around the time axis. The rate at which a steady-state condition is reached is largely dependent upon the transformer primary circuit time constant. That is L_M / R_S in Fig. 12-4b, where L_M is transformer magnetising inductance, and R_S represents copper loss and

other series primary circuit resistance. An analysis of Fig. 12-4b now follows to show this.

12-2-1 Circuit Analysis For Transient Effect

Fig. 12-4a shows the circuit used to analyse the effect of L_M and R_S on the time taken to correct for adverse initial values of flux and, hence, on the magnetising current transient decay time. Fig. 12-4b shows the equivalent circuit used to analyse Fig. 12-4a where

R_S is the sum of winding and source resistance,

L_S is the sum of the leakage and source inductance (if any),

R'_L is the reflected secondary load resistance; $R'_L = (N_P/N_S)^2 R_L$.

The core loss resistance is assumed to have the effect of reducing R'_L because it is effectively in parallel with it, and is neglected. From Fig. 12-4b, the following equations may be written:

$$i_P - i_M - i'_S = 0 \tag{12-2}$$

$$i'_S = \frac{v_P}{R'_L} \tag{12-3}$$

$$v_I - i_P R_S - v_{LS} - v_P = 0 \Rightarrow v_{LS} = v_I - i_P R_S - v_P \tag{12-4}$$

$$v_{LS} = L_S \frac{di_P}{dt} \Rightarrow \frac{di_P}{dt} = \frac{v_{LS}}{L_S} \tag{12-5}$$

$$\frac{di_P}{dt} = \frac{1}{L_S}[v_I - (R_S + R'_L)i_P + R'_L i_M] \tag{12-6}$$

$$v_P = L_M \frac{di_M}{dt} \Rightarrow \frac{di_M}{dt} = \frac{v_P}{L_M} \tag{12-7}$$

$$\frac{di_M}{dt} = \frac{R'_L}{L_M}(i_P - i_M) \tag{12-8}$$

Using the MAPLE symbolic computation package to solve the differential equations (12-6) and (12-8) results in an equation for i_M having the form shown in Eq. (12-9), where k_1, k_2 and k_3 are constants [see App. (12-1)]:

$$i_M(t) = v_I(k_1 + k_2 e^{-t/\tau_1} + k_3 e^{-t/\tau_2}) \tag{12-9}$$

$$\tau_1 = \frac{2aL_M}{R'_L(1+a+b+\sqrt{c})} = \frac{2a\tau_e}{1+a+b+\sqrt{c}} \tag{12-10}$$

$$\tau_2 = \frac{2aL_M}{R'_L(1+a+b-\sqrt{c})} = \frac{2a\tau_e}{1+a+b-\sqrt{c}} \tag{12-11}$$

$$a = \frac{L_S}{L_M}, \quad b = \frac{R_S}{R'_L}, \quad c = 1+2a+2b+a^2-2ab+b^2$$

and

$$\tau_e = \frac{L_M}{R'_L} \tag{12-12}$$

A steady-state value of i_M is reached when the second and third terms in Eq. (12-9) approach zero, i.e. as $t \to \infty$. An approximate steady-state condition may be deemed to have been reached after 3 τ_1 or 3 τ_2, whichever is longer. The normalised time-constants $\tau_{1n} = \tau_1 / \tau_e$ and $\tau_{2n} = \tau_2 / \tau_e$ are plotted in Fig. 12-5 as a function of a for b=1 and b=0.0001. At low values of a, τ_1 and τ_2 may be approximated as follows:

$$\tau_1 \approx \frac{a}{1+b}\tau_e = \frac{L_S}{R_S + R'_L} \tag{12-13}$$

$$\tau_2 \approx \frac{1+b}{b}\tau_e = \frac{L_M}{R'_S} \tag{12-14}$$

where

$$R'_S = \frac{R_S R'_L}{R_S + R'_L}$$

The exact range of a for which approximate τ_1 and τ_2 values are valid, may be judged from the dashed graphs in Fig. 12-5. From the figure, it can be seen that at low a, which represents practical situations where $L_S << L_M$, τ_2 is much larger than τ_1 (more than three orders of magnitude). This leads us to the conclusion that the L_M / R'_S time-constant may be used to quantify the time taken to reach steady-state operation, i.e. $\approx 3L_M / R'_S$. In practice, R_S is generally much smaller than R'_L;

therefore the time constant may be approximated by L_M / R_S as reasoned by Say [1, 2, 3]. A MATLAB program for plotting Fig. 12-5 is given in App. (12-2).

We now have a method of estimating the time taken to reach steady-state core flux operating condition in a PSPICE circuit simulation involving a transformer and/or inductor. The following example serves to verify the time-to-steady-state estimation. If a transformer using a 10 turn primary, a core type *ETD59* with $A_e = 3.68$ cm^2, $l_e = 13.9$ cm and $\mu_r = 2850$, is assumed for the circuit in Fig. 12-4, then the average value of L_M can be calculated as:

$$L_M = \frac{A_e}{l_e} N_P{}^2 \mu_o \mu_r \qquad (12\text{-}15)$$

$$L_M = \frac{3.68 \cdot 10^{-4}}{13.9 \cdot 10^{-2}} \cdot 10^2 \cdot 4\pi \cdot 10^{-7} \cdot 2850 \approx 0.95 \text{ mH}$$

With R_S values of 5, 10 and 15 Ω, τ_2 time-constant values of 0.19, 0.095 and 0.063 ms are obtained from $\tau_2 = \frac{L_M}{R_S}$.

To confirm these results, simulations of the circuit shown in Fig. 12-4a, with the same parameters as in the example above, were conducted using PSPICE. Fig. 12-6 shows the magnetising current for different R_S values, from which it may be shown that the times required for the current to settle are very close to the calculated ones obtained from the approximation above. Fig. 12-6 shows that, as R_S increases, the magnetising current approaches its steady-state value more rapidly. Fig. 12-7 shows the case where R_S is held constant, and different numbers of primary turns, N_P, are used to change the inductance, L_M. It can be seen that as L_M decreases the decay of the magnetising current increases. Time constants taken from Fig's 12-6 and 12-7 are compared with L_M/R_S time constants in Table (12-1).

App. (12-3) describes in full details how the time constant was calculated from simulation graphs, and why the value of 2850 was assigned for μ_r in Eq. (12-15). Irrespective of existing errors in calculating the time constants analytically and in simulation, as described in App. (12-3), and irrespective of L_M variations during

simulation, Table (12-1) shows good agreement between simulated and analytical results, and confirms the validity of the above time constant approximation for predicting the time required to reach steady-state conditions.

conditions	calculated τ_2 [ms]	τ_2 from PSPICE [ms]
R_S=5 , L_M=0.95 m	0.19	0.224
R_S=10 , L_M=0.95 m	0.095	0.11
R_S=15 , L_M=0.95 m	0.063	0.075
R_S=10 , L_M=0.95 m	0.095	0.11
R_S=10 , L_M=1.368 m	0.137	0.147
R_S=10 , L_M=1.862 m	0.186	0.2

Table (12-1) Calculated and simulated τ_2 time constants for different values of R_S and L_M

From the above, it is concluded that a relatively long time is required to reach the steady-state if it is assumed that all parasitic elements are properly added to the circuit. For example, if the switching frequency is more than 20 kHz, i.e. a switching period smaller than 50 μs, as is often the case in switching power supplies, a large number of switching cycles would have to be simulated before steady-state transformer operation is reached. In PSPICE it is impossible to simulate a few milli-seconds, if the waveforms are changing in hundreds of nano-seconds; this might take days of simulation time. Hence, it is imperative that a technique of pre-setting transformer core flux conditions be found.

12-2-2 Procedure For Rapidly Establishing Steady-State Flux

12-2-2-1 Single-phase transformer

In Fig. 12-2, when the voltage is at a sinewave peak, the flux is at a zero. Although initial values of the flux may not be set in the PSPICE non-linear transformer model, the possibility exists of setting the voltage at any value either by "delay" or "phase" parameters, and the voltage can be shifted such that it starts at a peak, to properly

coincide with a flux zero. Since the flux in the PSPICE transformer core always starts from zero, correct initial conditions may thus be rapidly established, and the core flux will hereafter increase or decrease according to the voltage. Using this procedure, exactly the right flux waveform is obtained, and the flux will be centred around zero as shown in Fig. 12-2. Voltage waveforms other than sinewaves should also be delayed, using similar reasoning as above, such that steady-state flux conditions may be rapidly established to model normal circuit operation without having to wait for transformer start-up transients to decay.

12-2-2-2 Three-phase transformer

In three-phase transformers, the simplest core is the three-limb cored type, where three voltages are applied to three windings on separate transformer core limbs. The applied voltage waveforms will be 120° out of phase. One of the voltages can be started at a peak as mentioned above; the other two will be at values lying at + and - 120° from the peak. To establish steady-state flux conditions in a three-phase transformer, the first voltage is delayed such that it starts at a peak value, the second voltage is not applied to the circuit until a peak (positive or negative) is reached. This is done using a switch which is turned "on" at the voltage peak as shown in Fig. 12-8. The switch then stays "on" for the rest of the simulation. The switch may be controlled by a pulsed voltage source model "Vpulse" or a piece-wise-linear voltage source "Vpwl", available in PSPICE. The flux in the third limb is similarly set up by applying the third phase voltage at a peak, as shown in Fig. 12-10.

The circuit in Fig. 12-9 allows the initialisation of steady-state flux conditions in core limbs to be simulated in PSPICE, where

V_1, V_2 and V_3 are the three-phase voltages,

V_{C2} and V_{C3} are the piece-wise-linear voltage sources to control the switches S_2 and S_3,

R_1 is very small and used to break the loop between a voltage source and an inductor, and

TX_1 is the three-phase transformer under test.

Fig. 12-10 shows the three-phase voltages and the corresponding flux.

12-3 MATLAB NON-LINEAR SINGLE-PHASE TRANSFORMER MODEL

12-3-1 Simplified Transformer Model

Transformer primary current, i_P, comprises a reflected secondary current, i'_S, and magnetising current, i_M, components, as shown in Fig. 12-11a. The magnitude of i'_S is determined by the secondary circuit impedance, and the magnitude of i_M is set by the transformer magnetising inductance, L_M, for any a.c. voltage level. L_M is fixed at transformer manufacture by the number of turns in the excited winding and the core geometry and material.

For a transformer connected to a simulated a.c. supply and resistive load as shown in Fig. 12-11a, a mathematical transformer model may be developed for use in a numerical equation solver computer package, such as MATLAB, which allows the electrical and magnetic transformer operation conditions to be computed. Primary and secondary voltage and current waveforms and core flux waveform are computed by solving transformer Eq's (12-16) to (12-21). This is performed by the MATLAB/SIMULINK simulations illustrated in Fig. 12-11b.

$$v_S = \frac{N_S}{N_P} v_P \tag{12-16}$$

$$i_S = \frac{v_S}{R_L} \tag{12-17}$$

$$i'_S = \frac{N_S}{N_P} i_S \tag{12-18}$$

$$i_M = \frac{1}{L_M} \int_0^t v_P \, dt + i_M(t=0) \tag{12-19}$$

$$\phi = \frac{1}{N_P} \int_0^t v_P \, dt + \phi(t=0) \tag{12-20}$$

$$i_P = i_M + i'_S \tag{12-21}$$

Voltage, current and flux waveforms for the following circuit and transformer parameters are given in Fig's 12-12a and 12-12b:

Sinewave source: $\hat{V}_I = 100$ V, $f_I = 100$ kHz, $\phi_I = 90°$

Transformer : $N_P = 20$, $N_S = 4$, $L_M = 5.32$ mH

Load : $R_L = 10\ \Omega$

12-3-2 Non-Linear Transformer Model

In the transformer model shown above, L_M was assumed to be constant. In fact, L_M is a non-linear component since it varies directly with the permeability of the core, μ_r, [see Eq. (12-22)] which is not constant but varies with core flux density as shown in Fig. 12-13:

$$L_M = \frac{A_e}{l_e} N_P{}^2 \mu_o \mu_r \qquad (12\text{-}22)$$

In Eq. (12-22), μ_o is the absolute permeability and equals $4\pi 10^{-7}$ H/m, and μ_r is the relative permeability. μ_r is responsible for the change in magnetising inductance with core flux density, B, and, hence, the primary voltage, v_P. Fig. 12-13 shows how the permeability of the core grade 3C85 changes with B. Therefore, to improve the model, the non-linear behaviour of L_M should be included in the model.

12-3-2-1 Specifying non-linear magnetising inductance

A non-linear magnetising inductance MATLAB model may be set up using a B-dependant μ_r function as shown in Fig. 12-14. This solves Eq's (12-22) to (12-25) to give i_M and B for a given excitation voltage waveform. A magnetic field intensity calculation block may be added to display the assumed B-H curve.

$$i_M = \frac{1}{L_M}\int v_P dt \tag{12-23}$$

$$B = \frac{\phi}{A_e} = \frac{1}{A_e N_P}\int v_P dt \tag{12-24}$$

$$H = \frac{N_P \cdot i_M}{l_e} \tag{12-25}$$

If, for instance, a core type ETD59 which has a 3C8 material grade, is used with the following parameters:

$A_e = 3.68$ cm^2, and $l_e = 13.9$ cm, and if $N_P = 20$, as in the example above, then:

$$L_M = \frac{3.68 \cdot 10^{-4}}{13.9 \cdot 10^{-2}} \cdot 20^2 \cdot 4\pi \cdot 10^{-7} \cdot \mu_r = 133 \cdot 10^{-8} \mu_r \tag{12-26}$$

When L_M was assumed constant, μ_r was assumed to be 4000. Therefore, L_M was calculated to be 5.32 mH. To include the changes of μ_r in L_M, we made use of the MATLAB "look-up table" function, where discrete values of this table are taken from Fig. 12-13 and shown in App. (12-4) [4].

Fig. 12-14 shows a non-linear inductor model for obtaining i_M, which takes into account L_M variations with B. Fig. 12-15a shows the magnetising current waveform, together with the flux waveform for the conditions shown below the figure. Fig. 12-15b shows how H changes with B for the model in Fig. 12-14. It is noticed from Fig. 12-15 that as B increases beyond 200 mT, L_M starts to decrease and the magnetising current increases rapidly. A very high current will flow if the input voltage is further increased, and the non-linear inductor or transformer core is driven into saturation.

12-3-2-2 Adding primary circuit inductance and resistance

In the previous model, when the flux density increases, μ_r is reduced and the magnetising current increases rapidly. However, the model does not correctly predict the effects of flux saturation. For example, if the input voltage is dc, the model still gives an output equals to $\frac{N_S}{N_P} v_P$. Practically, when μ_r starts to decrease at the knee

of the hysteresis loop, the change in the flux $d\phi/dt$ starts to decrease. Therefore, the output voltage decreases, as it is proportional to $d\phi/dt$.

In practice, the voltage source has an impedance; resistance plus inductance. Also, the transformer has leakage inductance and wire resistance. These affect the primary voltage, and hence the output voltage, when the primary current increases due to saturation. Fig. 12-16 shows a simplified equivalent circuit of a transformer (ignoring core losses), including source and primary impedance, where

R_S and L_S are the source resistance and inductance, respectively,

R_P and L_L are the primary and secondary wire resistance and leakage inductance,

L_M is the magnetising inductance,

i'_S is the secondary current reflected to the primary,

i_M is the magnetising current and

i_P is the primary current.

Further terms may now be added to the transformer model to better reflect practical circuit operation, such as primary circuit and winding resistance, and primary circuit and winding leakage inductance as shown in Fig. 12-16.

Referring to Fig. 12-16, the following may be written:

$$v_I = v_P + v_D = v_P + (R_S + R_P)i_P + (L_L + L_S)\frac{di_P}{dt} \qquad (12\text{-}27)$$

$$v_P = v_I - [(R_S + R_P)i_P + (L_L + L_S)\frac{di_P}{dt}] \qquad (12\text{-}28)$$

Eq. (12-28) can be solved as shown in Fig. 12-17, where "subsystem" block is described in Fig. 12-18.

The MATLAB non-linear transformer model in Fig. 12-17 is used to compute v_P, i'_S, i_M and i_P waveforms with the following parameters:

Transformer: $N_P = 20$, $N_S = 4$, $R_P = 0.1\ \Omega$, $L_L = 100$ nH, core type is ETD59 with $A_e = 3.68\ cm^2$, $l_e = 13.9$ cm and 3C8 material grade.

Primary circuit impedance: $R_S = 0.1\ \Omega$, $L_S = 100$ nH

Source: sinewave with $\hat{V} = 300$ V , $\omega = 2\pi f$, $f = 100$ kHz

Load resistance: $R_L = 10\ \Omega$

Fig. 12-19a shows the input voltage, v_I, and the primary voltage, v_P, while Fig. 12-19b shows i'_S, i_M and i_P. Since R_P, R_S, L_L and L_S are small and no saturation occurs, the voltage drop across these impedances is very small, and the primary and input voltages are identical.

If the load is increased from $R_L = 10\ \Omega$ to $R_L = 2\ \Omega$, and L_L is increased from 100 nH to 5 μH, Fig. 12-20 will be obtained. Comparing Fig's 12-19 and 12-20, it is evident that a greater difference exists between v_P and v_I. A noticeable phase shift is now also seen between the two voltages v_P and v_I, i.e. v_P lags v_I because of the inductive primary circuit impedance. Fig. 12-20b shows the instantaneous values of i'_S, i_M and i_P, from which it can be seen that i'_S, and, hence, i_P become very large, while i_M remains relatively unchanged.

To prove that the model is able to show saturation, the effective area of the core has been reduced to increase the flux density, B, beyond the saturation value. Therefore, A_e was decreased from 3.68 cm^2 to 3.1 cm^2 and the frequency was reduced from 100 kHz to 20 kHz, and Fig. 12-21 was obtained. From Fig. 12-21b it can be noticed that at the time about 1.2 μs, i_M increases rapidly to about 23 A, because of saturation since L_M starts to decrease. This in turn, increases i_P which results in reduction in v_P as shown in Fig. 12-21a, and reduction in i'_S as it is proportional to v_P.

Although the model developed does not induce hysteresis, it can easily model all transformer conditions. Also, since this model deals with instantaneous values, it accepts any input voltage such as square wave, with any duty-ratio, since there is no restrictions on the shape of the input voltage. Furthermore, it accepts any load if an equation relating i_S to v_S is found. App. (12-5) shows some load configurations, the equations relating i_S to v_S, and how it can be implemented in MATLAB. These equations should replace the $1/R_L$ block in Fig. 12-18. Any secondary leakage

inductance, if any, can be added in series with load inductance. Fig. 12-22 shows some waveforms of voltages and currents when a square wave input voltage is applied to the transformer as shown in Fig. 12-22a. The load in this circuit was a pure inductive load of 100 μH. Higher voltage will saturate the core as can be seen from Fig. 12-22b. Fig. 12-22d shows the difference, $v_D = v_I - v_P$, because of the high primary impedance.

12-3-2-3 Using the model

Fig. 12-23a shows the complete MATLAB non-linear single-phase transformer model, where:

v_I is the input voltage,

v_S is the output voltage ,

R_S is an optional constant which represents any source and/or primary winding resistance. It can be left unconnected if a zero resistance is assumed,

L_S is an optional leakage and / or source inductance. It can also be left unconnected if it is assumed to be zero,

i_S is the secondary current, where the load should be connected between v_S and i_S [see App. (12-5)]. In case of resistive load, R_L, a gain of $1/R_L$ should be connected between these two points,

i_p , i_M are the primary and magnetising currents, and are taken out only for measurements and should not be connected.

The secondary winding resistance and leakage inductance can be included exactly the same way as in the primary. Alternatively, they can be included in the primary resistance and inductance.

A generalised MATLAB transformer model has been created for use in power-electronic circuit simulation and has been reduced to a simple sub-circuit schematic called NLSPT (Non-Linear Single-Phase Transformer), as shown in Fig. 12-23b.

CHAPTER TWELVE REFERENCES

1. M.G. Say, "The performance and design of alternating current machines", Pitman Paperbacks, Bath, 1958.
2. M.G. Say, "Introduction to the unified theory of electromagnetic machines", Pitman Publishing, Bath, U.K., 1971.
3. M.G. Say, "Alternating current machines", Longman Scientific & Technical, Fifth Edition, Essex, U.K., 1983.
4. "Soft Ferrites", Book MA01, Philips, 1993.

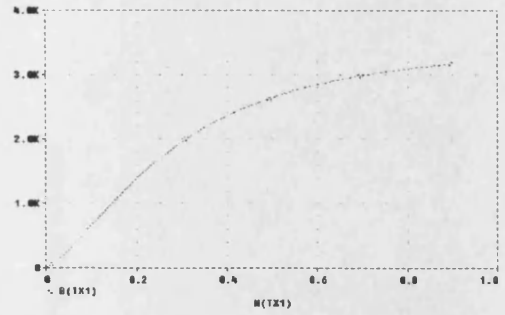


Fig. 12-1 Magnetising curve

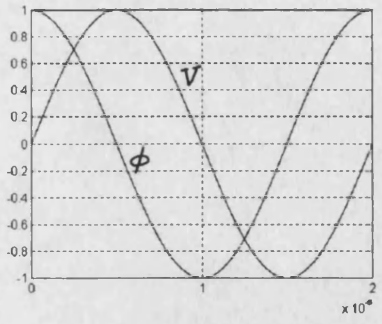


Fig. 12-2 Sinewave excitation voltage and corresponding core flux

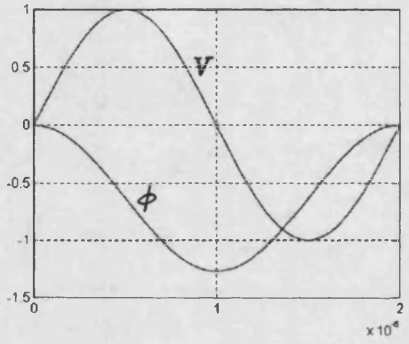
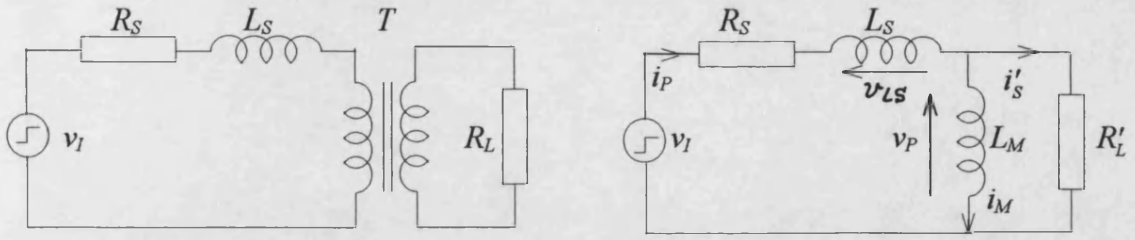


Fig. 12-3 Sinewave excitation voltage and corresponding core flux as obtained in PSPICE model



(a) (b)

Fig. 12-4 (a) Transformer circuit and (b) simplified equivalent circuit to estimate time taken to reach steady-state flux condition

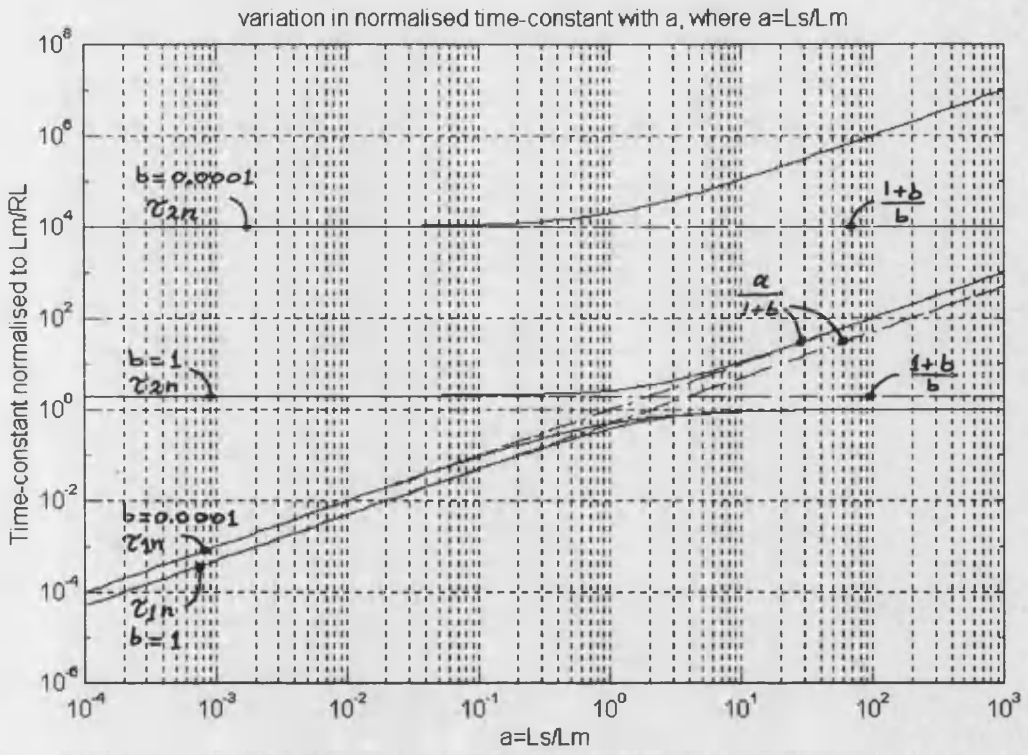


Fig. 12-5 Normalised time constants variations with L_s / L_M

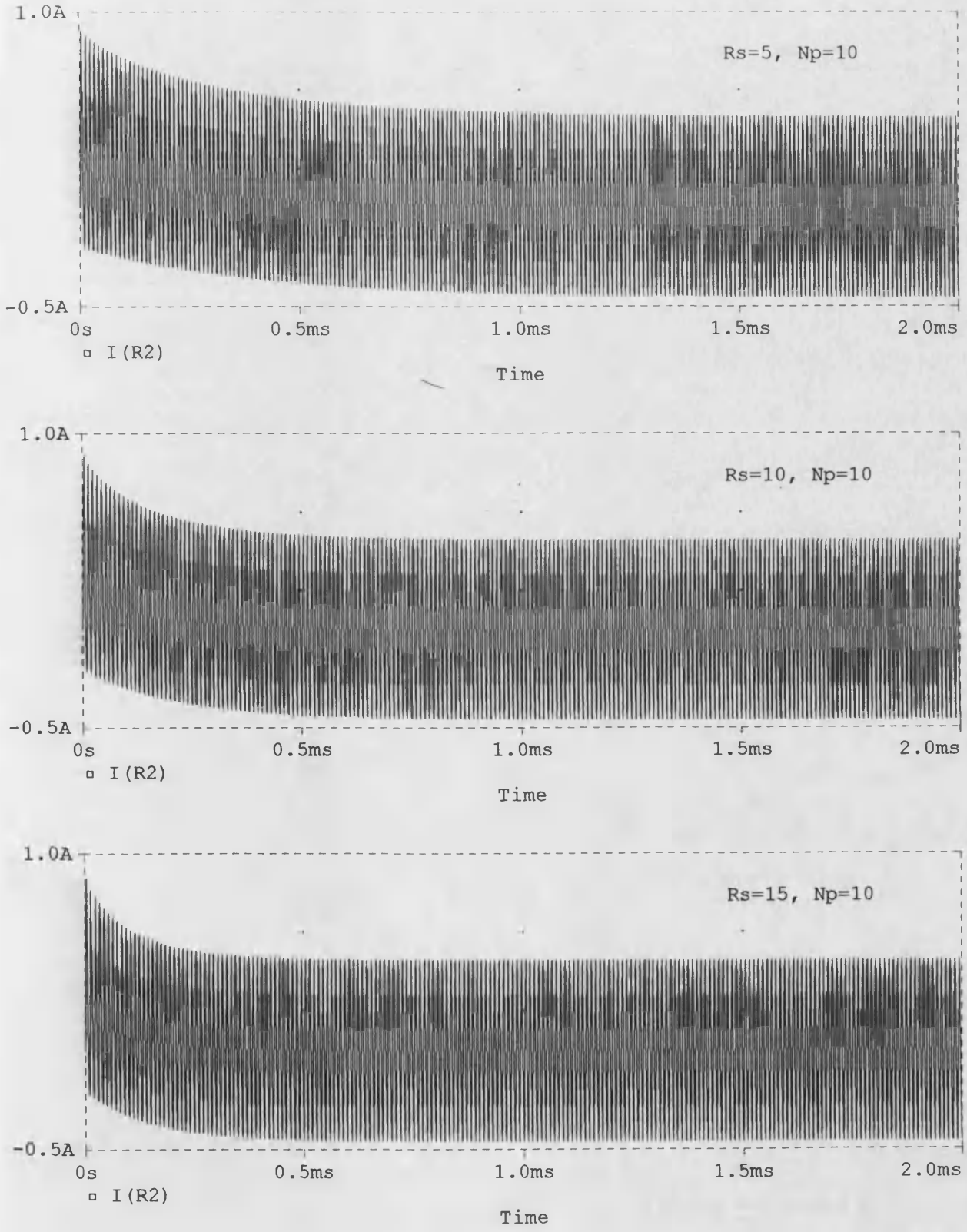


Fig. 12-6 Initial magnetising current for different R_S values as obtained from PSPICE

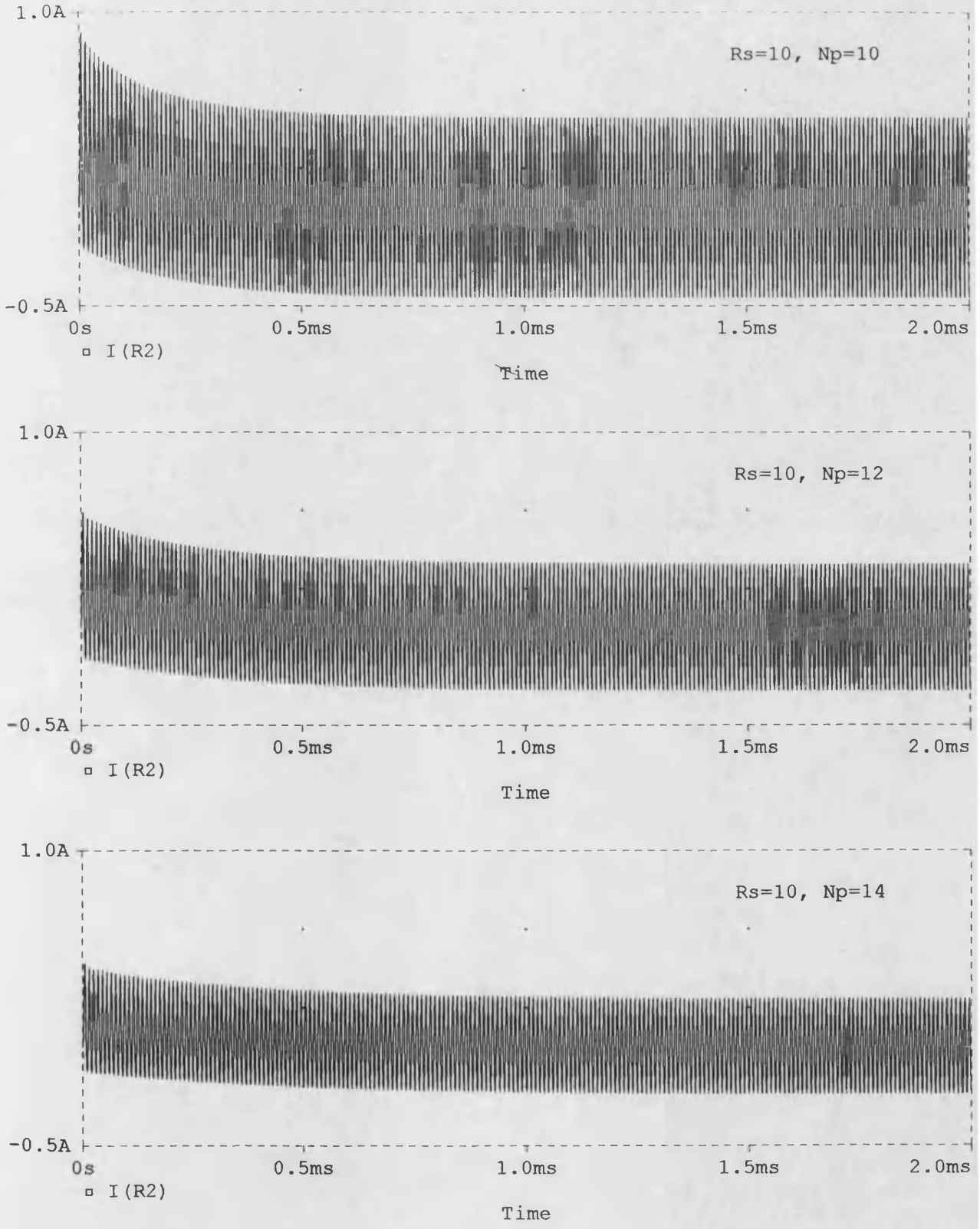
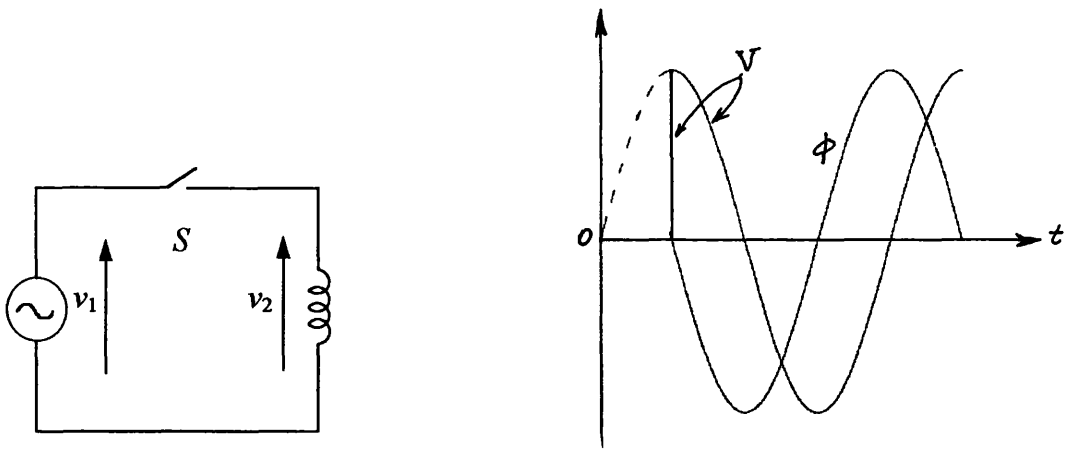


Fig. 12-7 Initial magnetising current for different L_M values as obtained from PSPICE



(a) (b)

Fig. 12-8 (a) A circuit to switch at a voltage peak, and (b) the resulting voltage and flux waveforms.

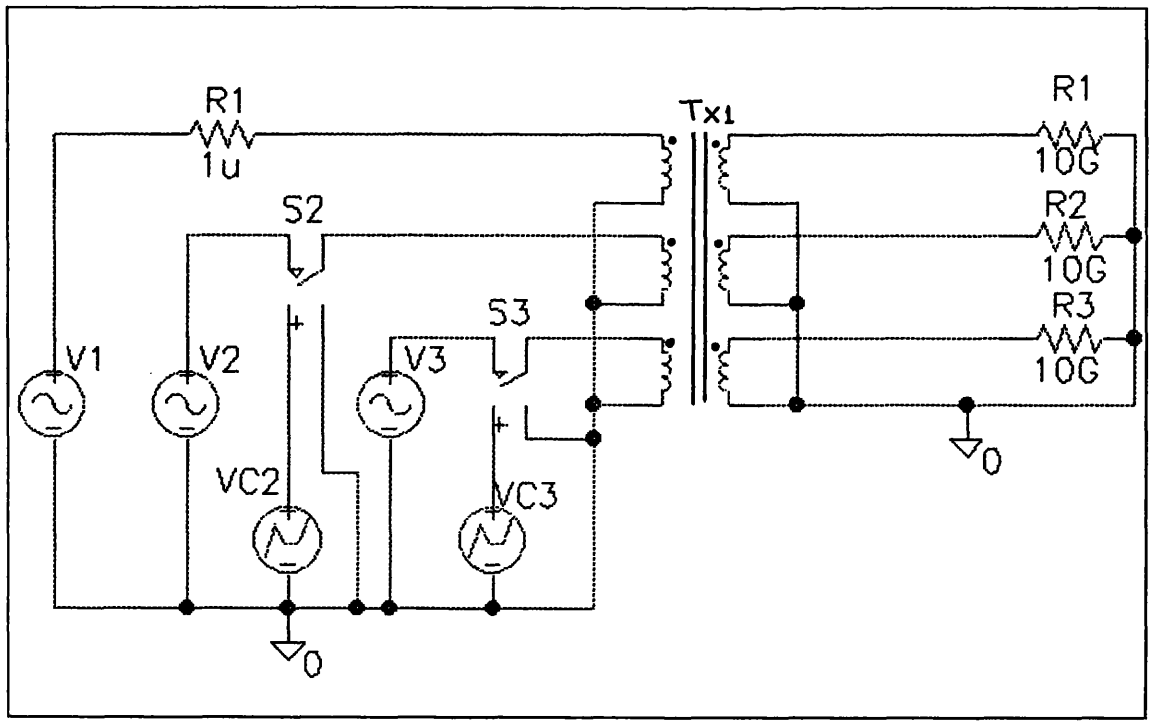


Fig. 12-9 A circuit to simulate flux pre-setting in a three-phase transformer

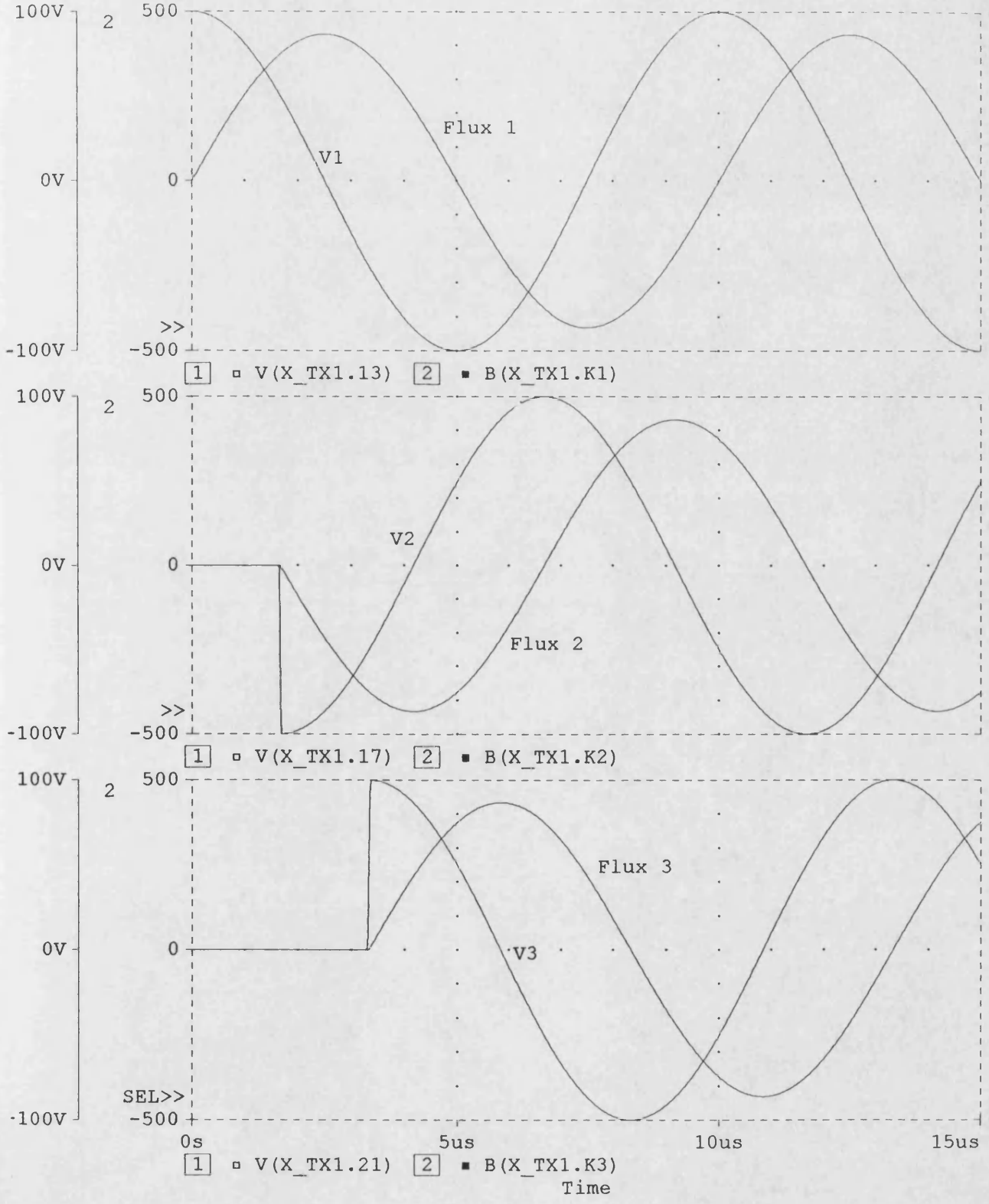
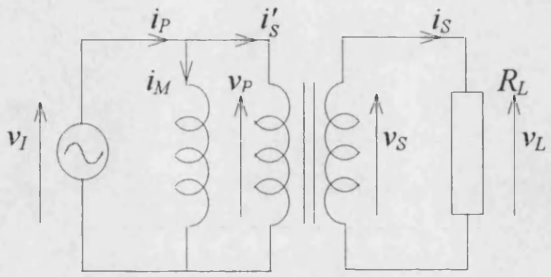
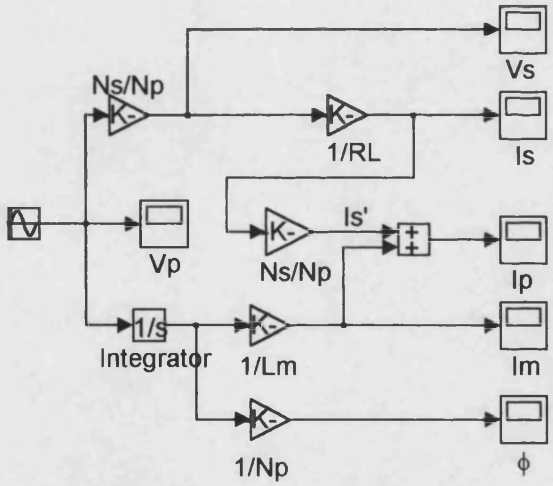


Fig. 12-10 Voltages and the corresponding flux waveforms in a three-phase transformer shown in Fig. 12-9

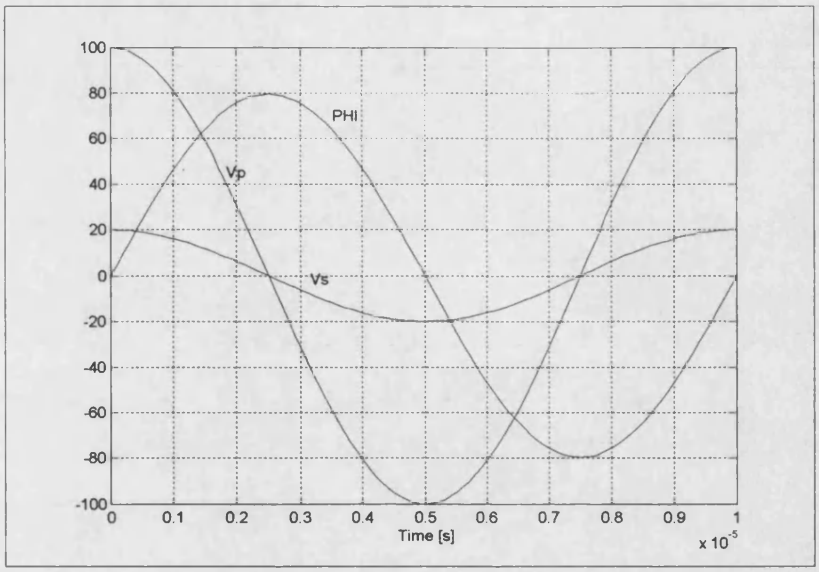


(a)

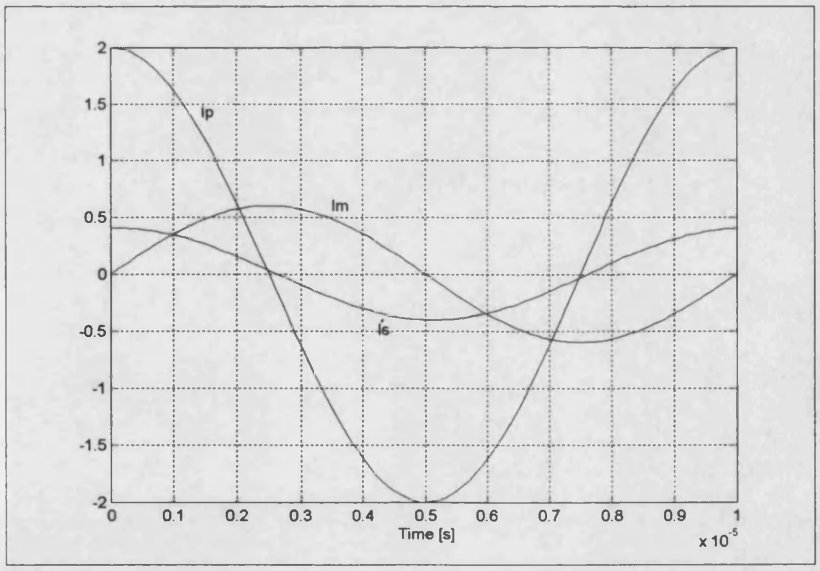


(b)

Fig. 12-11 (a) Transformer circuit and (b) the simplified MATLAB transformer model



(a) v_P, v_S and $\phi \cdot 10^7$



(b) i_P, i'_S, and $i_M \cdot 20$

Fig. 12-12 Waveforms for the simplified transformer model in Fig. 12-11

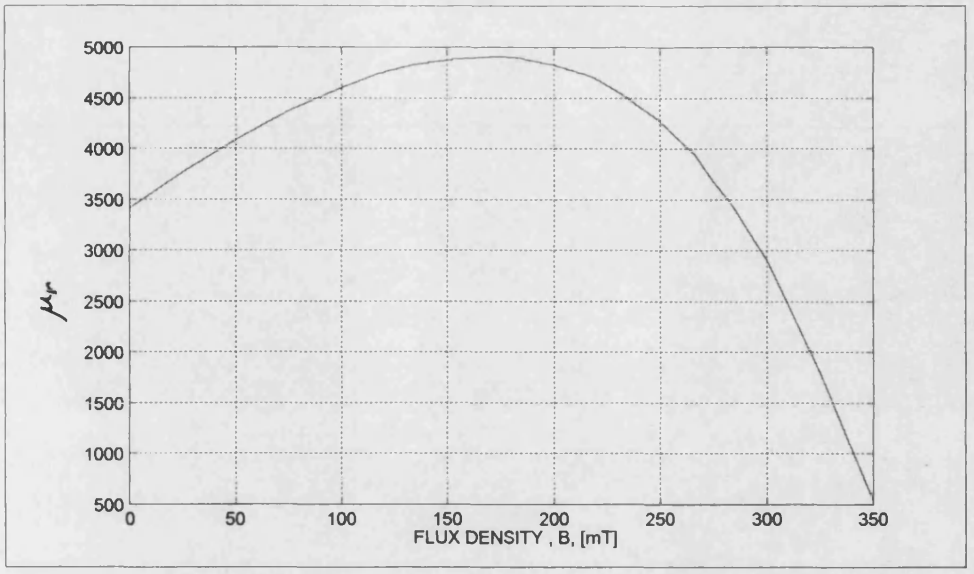


Fig. 12-13 μ_r versus flux density, B, for 3C85 grade ferrite core material

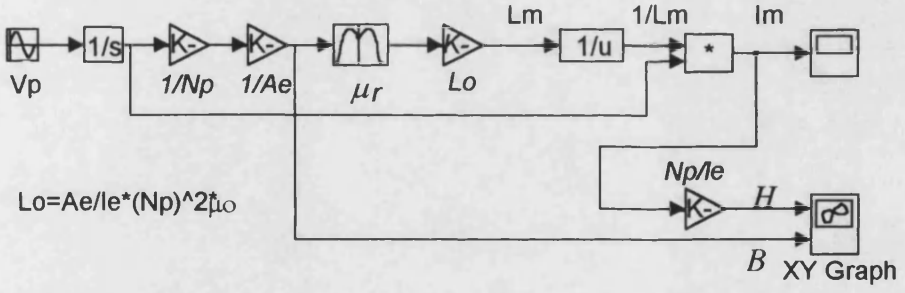
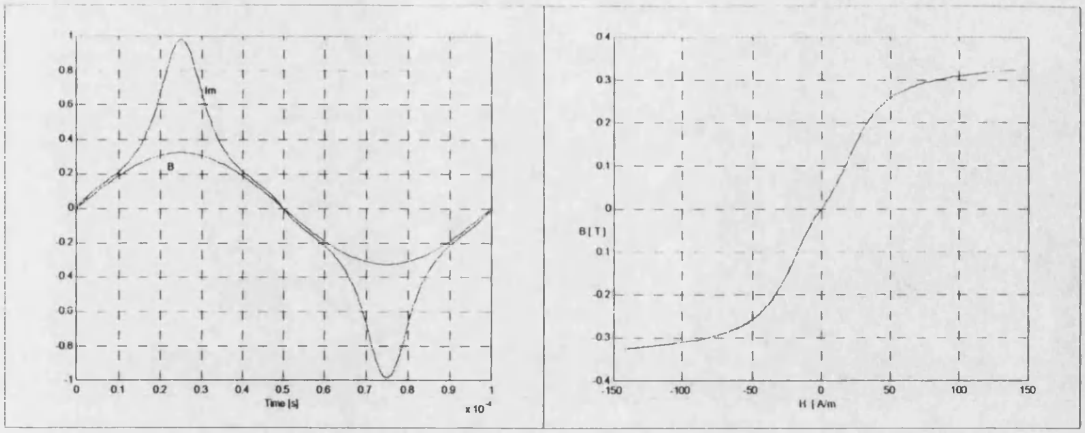


Fig. 12-14 Magnetising inductance and current models



(a) Magnetising current considering L_M variations with B

(b) Flux density, B, versus magnetic field, H

Fig. 12-15 (a) Magnetising current and flux density, and (b) B-H loop for a sinewave input voltage: $\hat{V} = 160$ V, $f = 10$ kHz

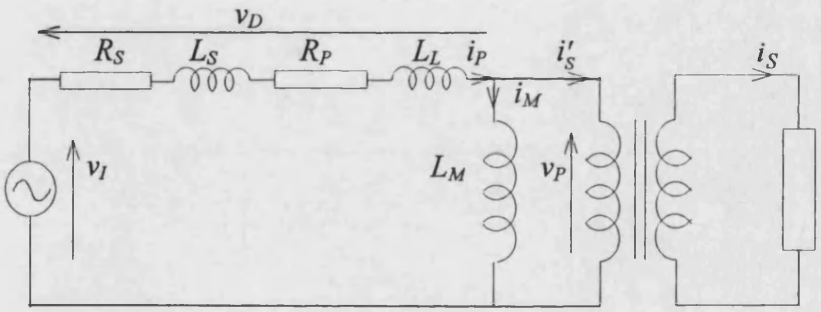


Fig. 12-16 Transformer equivalent circuit taking into account primary and source impedances

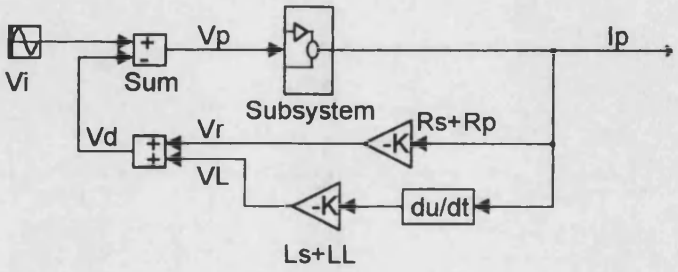


Fig. 12-17 Calculating v_P from v_I and i_P

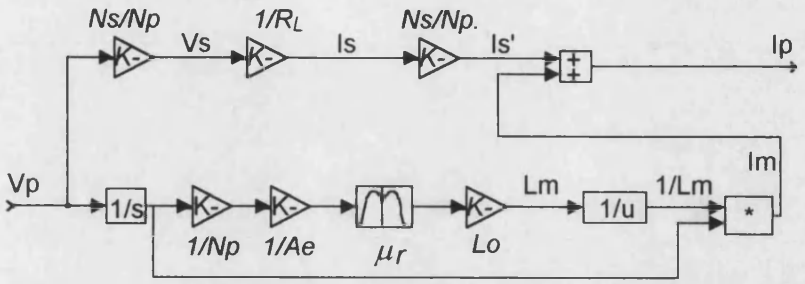
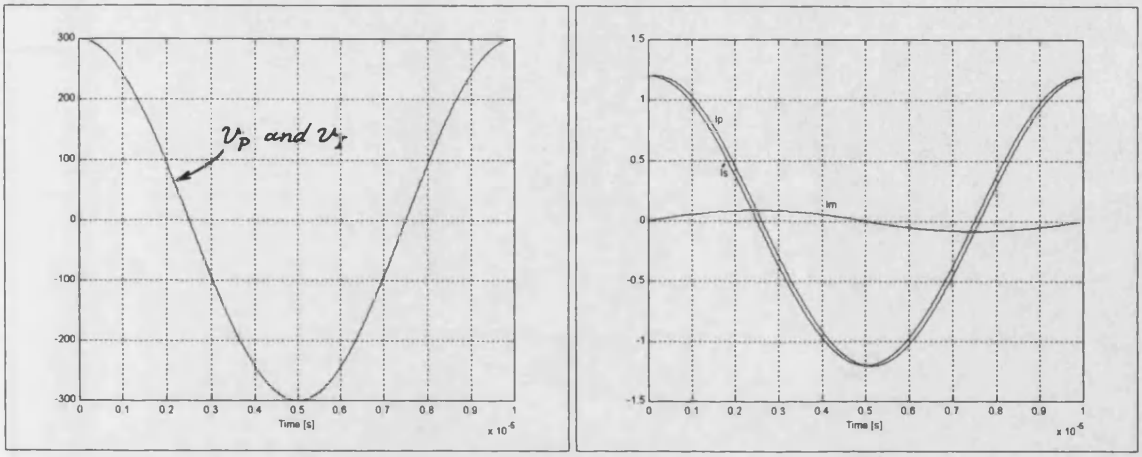
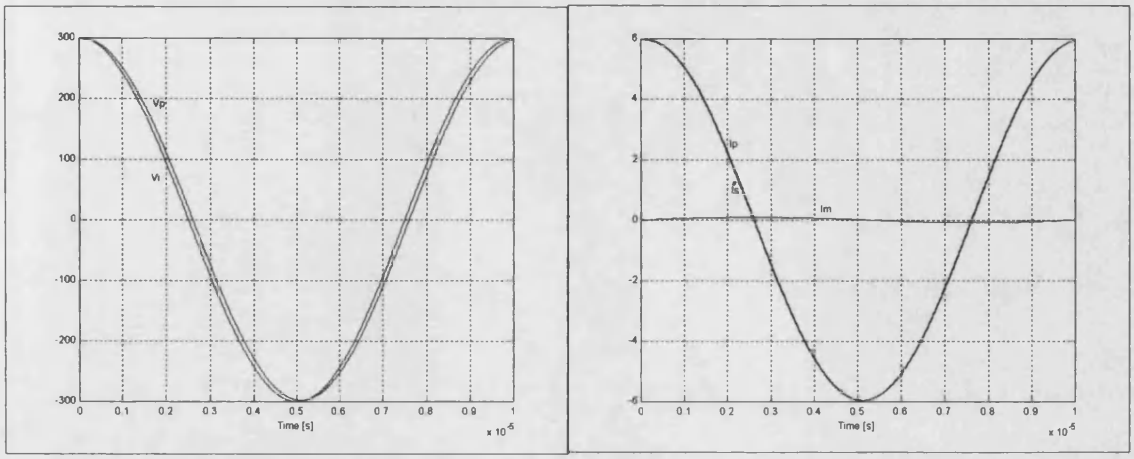


Fig. 12-18 Calculating i_P, i'_S and i_M from v_P



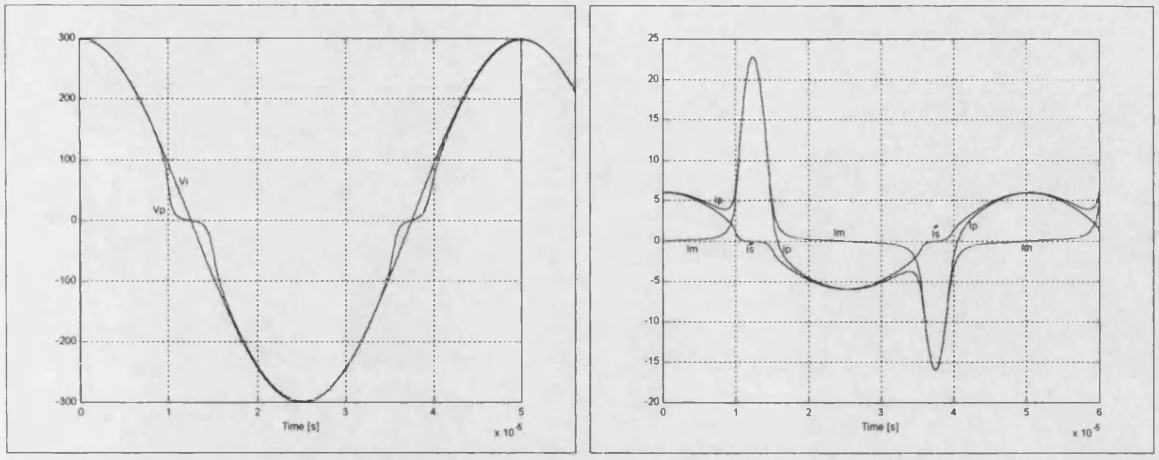
(a) (b)

Fig. 12-19 Waveforms for a sinewave input voltage: $\hat{V}$ = 300 V , R_L = 10 Ω, L_L = 100 nH, A_e = 3.68 cm^2, f = 100 kHz



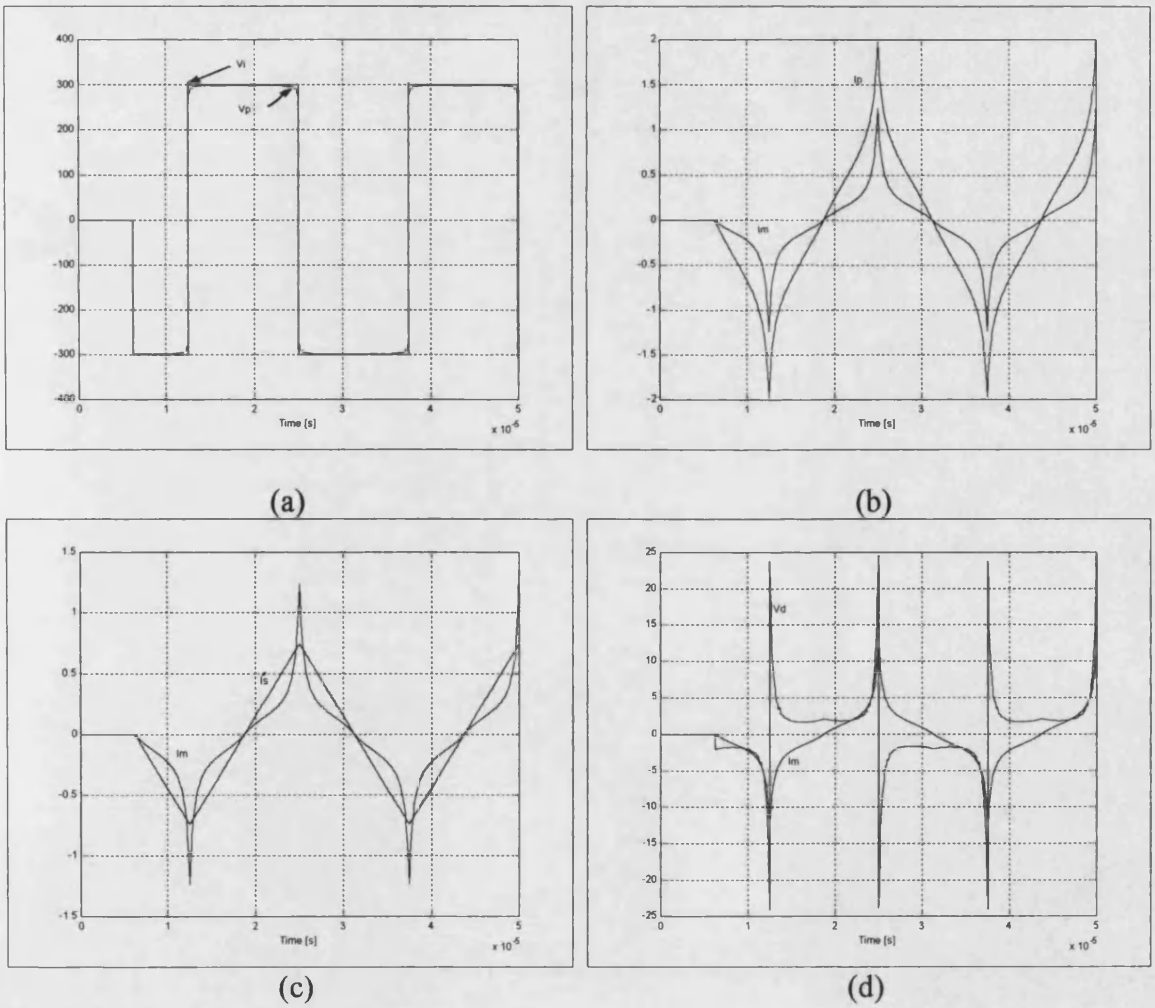
(a) (b)

Fig. 12-20 Waveforms for a sinewave input voltage: $\hat{V}$ = 300 V , R_L = 2 Ω, L_L = 5 μH, A_e = 3.68 cm^2, f = 100 kHz



(a) (b)

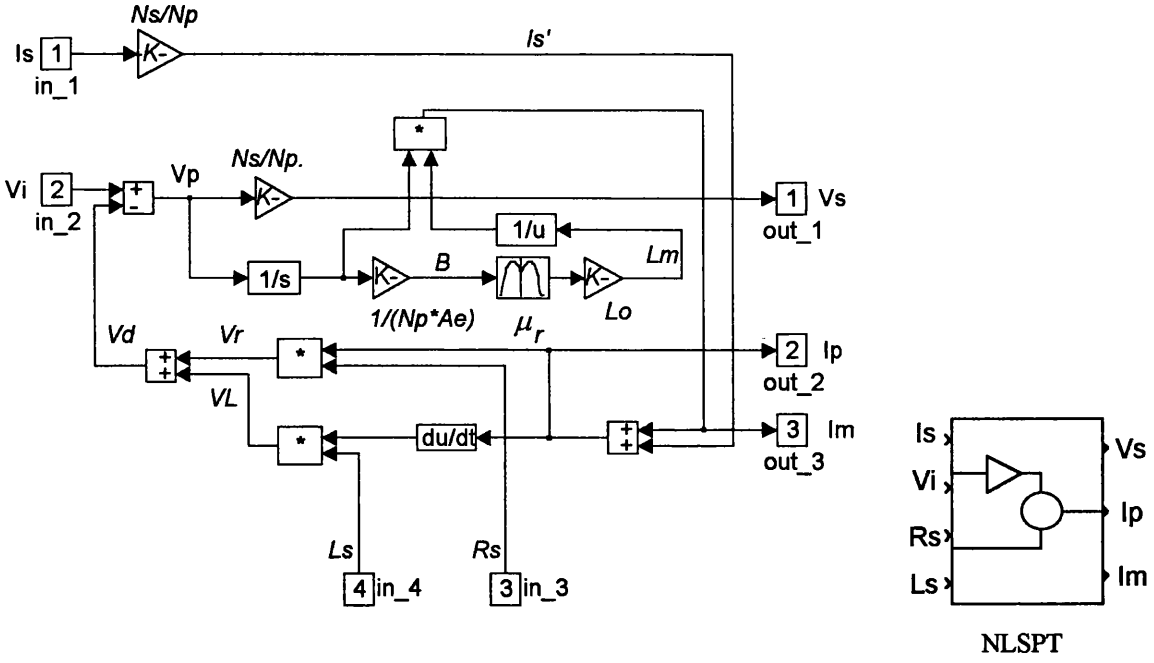
Fig. 12-21 Waveforms for a sinewave input voltage: $\hat{V} = 300$ V, $R_L = 2\ \Omega$, $L_L = 5$ μH, $A_e = 0.5$ cm^2, $f = 20$ kHz



(a) (b)

(c) (d)

Fig. 12-22 Waveforms for a square wave input voltage: $\hat{V} = 300$ V, load = 100 μH, $L_L = 100$ μH, $f = 20$ kHz, $A_e = 2.8$ cm^2



(a) (b)

Fig. 12-23 (a) The complete non-linear single-phase MATLAB transformer model and (b) its symbol

MATLAB TRANSFORMER-ISOLATED DC/DC CONVERTER MODELING

13-1 INTRODUCTION

In the previous chapter, the development of a non-linear single-phase transformer model was discussed. This will now be used to simulate the operation of several transformer-isolated dc/dc converter topologies such as single-ended forward converter and flyback converter.

The philosophy of the simulation is to set up a set of equations that describe the behaviour of the system when the power switch is "on". When the switch is "off", another set of equations should be set up, taking into consideration the interruption of the transformer magnetising current. Parameter values from one state of operation should be transferred to the next state of operation, and used as initial conditions for this state. The equivalent circuit for each state will be drawn to facilitate understanding the model.

As mentioned earlier, a full understanding of the function of the simulated circuit including the transformer operation, and the equations that describe each state of operation are essential in such modeling techniques. For details on dc/dc converters operation, refer to chapters 2 and 3.

13-2 MODELING A CIRCUIT WITH A PURE RESISTIVE LOAD

At first, the simple circuit shown in Fig. 13-1a is modeled, where two states of operation can be distinguished.

13-2-1 The Switch is "on"

In this case, the equivalent circuit is as shown in Fig. 13-1b, where the following equations can be written:

$$i_P = i_M + I'_L \tag{13-1}$$

$$i_M = \frac{1}{L_M}\int v_P \, dt \tag{13-2}$$

$$I'_L = \frac{v_P}{R'_L} \tag{13-3}$$

where

$$R'_L = R_L\left(\frac{N_P}{N_S}\right)^2 \tag{13-4}$$

Eq's (13-1), (13-2) and (13-3) contain three unknowns: i_P, i_M and I'_L, and can be solved easily as will be shown shortly.

13-2-2 The Switch is "off"

In this case, the equivalent circuit transfers to that shown in Fig. 13-1c, where V_{IN} is disconnected from the circuit and only R'_L is connected in parallel with L_M. Energy has been stored in L_M during the first state and is going to be dissipated in R'_L.
At the instant of turn-off, i_M has a value $I_{M(max)}$ which is the last value from the previous state, and decreases exponentially according to the following equation:

$$i_M = I_{M(\max)} e^{-t/\tau} \tag{13-5}$$

where

$$\tau = \frac{L_M}{R'_L} = \frac{L_M}{R_L}\left(\frac{N_S}{N_P}\right)^2 \tag{13-6}$$

The magnetising current given in Eq. (13-5) should produce the same voltage v_P that generates this current. If the equation :

$$v_P = L_M \frac{di_M}{dt} \tag{13-7}$$

is simply used to obtain v_P, the resulting v_P does not produce the same i_M, and no solution for Eq's (13-2) and (13-7) is found. The reason for this is that L_M is not constant but varies with time. Therefore, Eq. (13-7) should be modified taking into consideration L_M variations as follows:

$$v_P = \frac{d(L_M i_M)}{dt} \tag{13-8}$$

From Fig. 13-1c, it can be written:

$$v_P = \frac{d(L_M i_M)}{dt} = -R'_L i_M \tag{13-9a}$$

$$\frac{d(L_M i_M)}{dt} + R'_L i_M = 0 \tag{13-9b}$$

which can be rewritten as:

$$i_M(t)\frac{dL_M(t)}{dt} + L_M(t)\frac{di_M(t)}{dt} + R'_L i_M(t) = 0 \tag{13-10}$$

Using MAPLE software to solve Eq. (13-10) gives:

$$i_M(t) = Ke^{-\int \frac{\frac{dL_M(t)}{dt}+R'_L}{L_M(t)}dt} \tag{13-11}$$

Eq. (13-11) is used to calculate the magnetising current (which is the same as the load current in this case) during the second state of operation.

In Eq. (13-11), if L_M(t) is constant, then $\frac{dL_M(t)}{dt} = 0$, and the current becomes:

$$i_M(t) = Ke^{-\frac{R'_L}{L_M}t} = Ke^{-t/\tau} \tag{13-12}$$

At $t = 0$, $i_M(t) = I_{M(\max)}$ which yields $K = I_{M(\max)}$. Therefore,

$$i_M(t) = I_{M(\max)}e^{-t/\tau} \tag{13-13}$$

which is the same as Eq. (13-5). However, if L_M(t) changes with time, Eq. (13-5) is no longer valid and Eq. (13-11) should be used instead.

The constant K may be obtained from Eq. (13-11) where at $t = 0$, $i_M(t) = I_{M(\max)}$. Substituting this in Eq. (13-11) gives:

$$I_{M(\max)} = Ke^{-\int \frac{\frac{dL_M(t)}{dt}+R'_L}{L_M(t)}dt}\Bigg|_{t=0} \tag{13-14}$$

$$K = I_{M(\max)}e^{\int \frac{\frac{dL_M(t)}{dt}+R'_L}{L_M(t)}dt}\Bigg|_{t=0} \tag{13-15}$$

13-2-3 Model Description

In the last two sections, the equations for each equivalent circuit corresponding to the various states of operation of the modeled circuit were derived, and now ways of solving these equations in MATLAB will be considered.

Eq's (13-11) and (13-15) may be realized as shown in Fig. 13-2, where the "S" block represents the power switch in the circuit with a step function as the controlling signal. From the figure, it can be seen that K follows Eq. (13-15) as long as the control signal is zero (the power switch is "on"). When the control signal takes a positive value (the power switch is "off"), K takes the last value defined by Eq. (13-15) which stays constant as long as the switch is "off". This value is used to calculate v_P using Eq. (13-9a) when the switch is off.

Fig. 13-3 shows the complete circuit model which may include values of primary and secondary winding resistance if known, and also leakage inductance as described in Ch. 12, turns ratio, core parameters, etc.

Fig. 13-4a depicts the i_M and v_P waveforms obtained using the model in Fig. 13-3, whereas Fig. 13-4b depicts the same waveforms obtained using a PSPICE model with the same parameters. In the figure, a small difference between the magnetising currents is evident. This is due to using the "average B/H" curve in the model instead of using the B/H hysteresis loop.

The time taken by PSPICE to simulate 20 μs at a tolerance of 0.1% is 26 s, while that required by MATLAB for the same parameters and at the same conditions is only 4 s.

13-3 SINGLE-ENDED FORWARD CONVERTER

Fig. 13-5 shows a single-ended forward converter, together with the equivalent circuits for the two states of operation, when the power switch is "on" and "off". For each state, the following sets of equations can be written:

13-3-1 The Switch is "on"

$$v_R = -\frac{N_R}{N_P} v_P \tag{13-16}$$

$$v_S = \frac{N_S}{N_P} v_P \tag{13-17}$$

$$i_M = \frac{1}{L_M} \int v_P \, dt \tag{13-18}$$

$$i_P = i_M + I'_L = i_M + \frac{N_S}{N_P} I_L \tag{13-19}$$

13-3-2 The Switch is "off"

$$v_P = -\frac{N_P}{N_R} v_R \tag{13-20}$$

As far as the magnetising current is concerned, two cases can be distinguished in this state:

13-3-2-1 $i'_M > 0$

$$v_R = V_{IN} + V_D \tag{13-21}$$

$$v_P = -\frac{N_P}{N_R}(V_{IN} + V_D) \tag{13-22}$$

$$v_S = \frac{N_S}{N_P} v_P \tag{13-23}$$

$$v_R = -\frac{d(L_M i'_M)}{dt} \tag{13-24a}$$

which gives:

$$-\int v_R \, dt + c = L_M i'_M \tag{13-24b}$$

$$i'_M = \frac{1}{L_M}(-\int v_R \, dt + c) = \frac{-v_R t + c}{L_M} \tag{13-24c}$$

where i'_M is the reflected magnetising current to the reset winding.

At $t = 0$, $i'_M = i'_{M(\max)}$ and Eq. (13-24c) gives:

$$i'_{M(\max)} = \frac{c}{L_M} \tag{13-25a}$$

$$c = L_M i'_{M(\max)} \tag{13-25b}$$

Therefore, $$i'_M = i'_{M(\max)} - \frac{v_R t}{L_M} \qquad (13\text{-}26)$$

13-3-2-2 $i'_M = 0$

When the magnetising current reaches zero, all winding voltages become zero. This is reached at the time defined by:

$$t = L_M i'_{M(\max)} / v_R \qquad (13\text{-}27)$$

13-3-3 Model Description and Discussion

Fig. 13-6 shows how the equations for both states may be implemented in MATLAB, where as in the previous model, a step function is used as the switch control signal to change between both states. Fig. 13-7 depicts i_M and v_P waveforms obtained using this model together with the same waveforms obtained for one cycle with a PSPICE model.

PSPICE model results show that number of cycles required to reach the steady-state operation for the simulated circuit is 10 cycles, which has been reached in only one cycle in MATLAB. The time taken to reach the steady-state in PSPICE is 150 s, while that needed in MATLAB is only 3 s.

13-4 FLYBACK CONVERTER

Fig. 13-8 shows a flyback converter, together with the equivalent circuits for the two states of operation, when the power switch is "on" and "off". For the equivalent circuit, the following sets of equations apply:

13-4-1 The Switch is "on"

$$i_M = i_P = \frac{1}{L_M}\int v_P \, dt \tag{13-28}$$

$$v_P = v_{IN} \tag{13-29}$$

$$i_S = 0 \tag{13-30}$$

13-4-2 The Switch is "off"

$$v_S = V_O + V_D \tag{13-31}$$

$$i_M = -\frac{1}{L_M}\int v'_S \, dt + c \tag{13-32}$$

$$i_M = \frac{-(V_O + V_D)\frac{N_P}{N_S}}{L_M} t + c \tag{13-33}$$

At $t = o$, $i_M = i_{M(\max)} = I_{M(\max)} \frac{N_P}{N_S}$, which yields:

$$i'_M = \frac{N_P}{N_S} I_{M(\max)} - \frac{(V_O + V_D)\frac{N_P}{N_S}}{L_M} t \tag{13-34}$$

Two states can be distinguished:

<u>13-4-2-1</u> $i'_M > 0$

$$v_P = -v_S \frac{N_P}{N_S} = -(V_O + V_D)\frac{N_P}{N_S} \tag{13-35}$$

<u>13-4-2-2</u> $i'_M = 0$

$$\begin{aligned} v_P &= v_S = 0 \\ i_P &= i_S = 0 \end{aligned} \tag{13-36}$$

13-4-3 Model Description

Fig. 13-9 shows the MATLAB model for the flyback converter shown in Fig. 13-8a, where V_O is the output voltage and V_D is the forward voltage drop across the rectifier. S_3 is used to hold the maximum magnetising current which is used to calculate the time at which the magnetising current reaches zero; S_1 changes the primary voltage from the input voltage to that reflected from the secondary when the switch turns "off"; and S_2 is used to force the voltage across the primary and secondary windings to have zero value when the magnetising current reaches zero.
Fig. 13-10a shows the simulated primary voltage and magnetising current during both operating states which were obtained using the model. All other parameters, such as primary and secondary current and output voltage, can be examined in the same way.
It can be seen from Fig. 13-10 that the MATLAB model gives typical waveforms and does not take into consideration the changes in voltage drop on the rectifying diode according to the current and the changes in the output voltage, which affect the magnetising current in this type of converters.
Fig. 13-10b shows the primary voltage and magnetising current as obtained using a PSPICE model with the same parameters and operating under the same conditions. The results agree quite well. The time taken to simulate the circuit in PSPICE is 71 s, while that required to simulate the circuit in MATLAB is only 3 s.

13-5 CONCLUSION

As discussed in the previous sections, MATLAB can be used to simulate transformer-isolated dc/dc converters. It is very fast and does not suffer from the difficulties that exist in PSPICE such as non-convergence problems.
MATLAB can only give more idealized waveforms which largely exclude practical device effects. If accurate results are required, considerable time should be spent to set up the required equations.

MATLAB dc/dc converter modeling requires a full understanding of the operation of the converter including non-linear behavior of the isolating transformer and all equations that describe the behavior of the circuit.

The inclusion of the core hysteresis effect in the model is still difficult due to the difficulty in obtaining a single equation which describes the complete hysteresis loop.

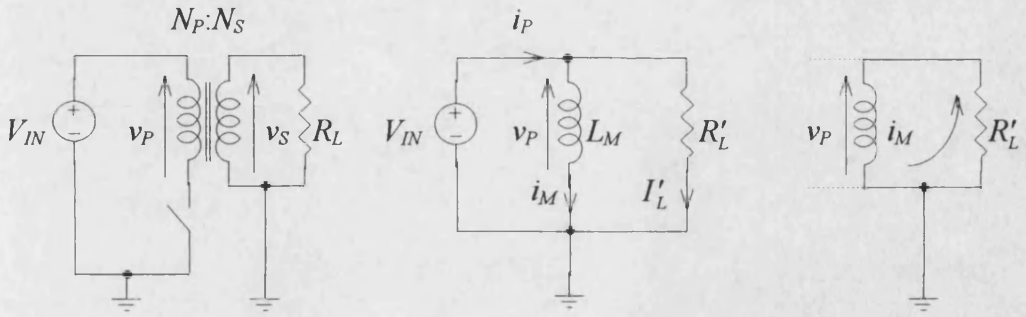


Fig. 13-1 a) Simple circuit, b) the equivalent circuit at switch turn-on and c) the equivalent circuit at switch turn-off

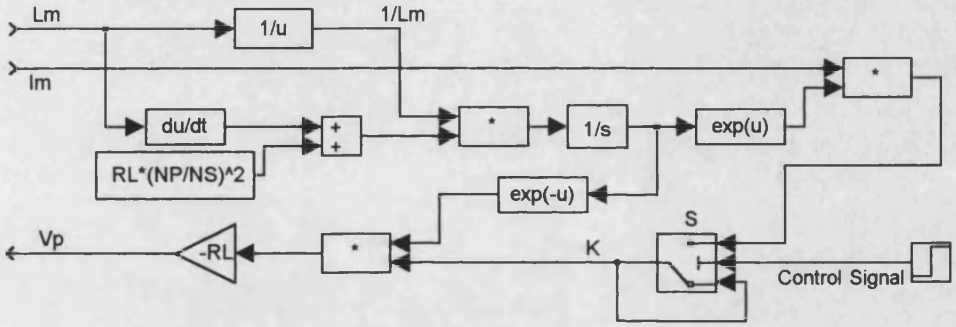


Fig. 13-2 Calculating K, i_M and v_P

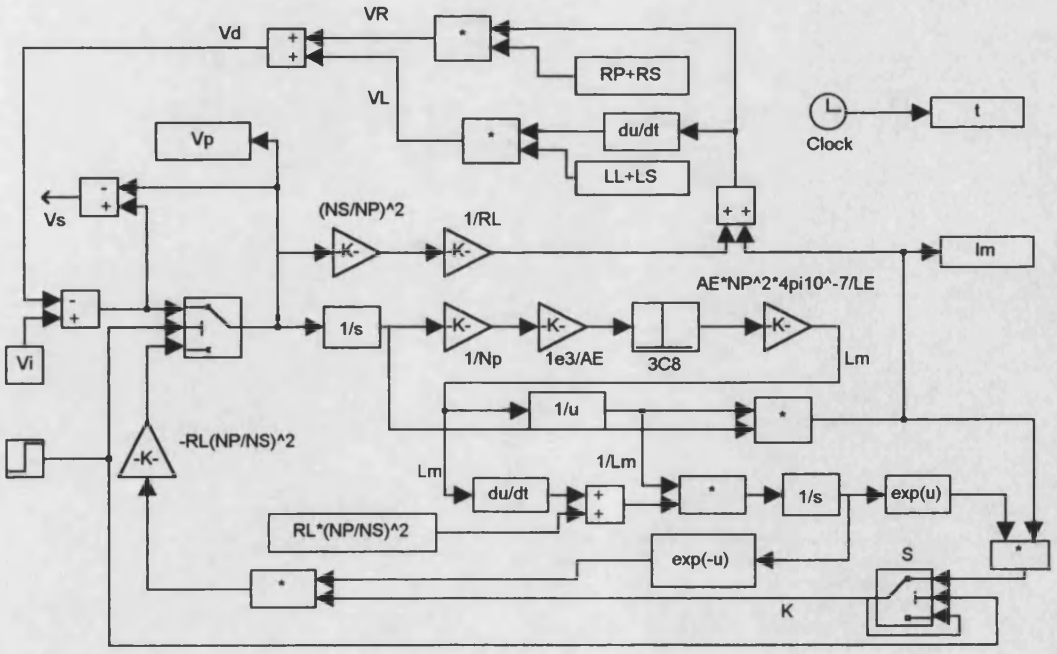


Fig. 13-3 The complete circuit model for a pure resistive load

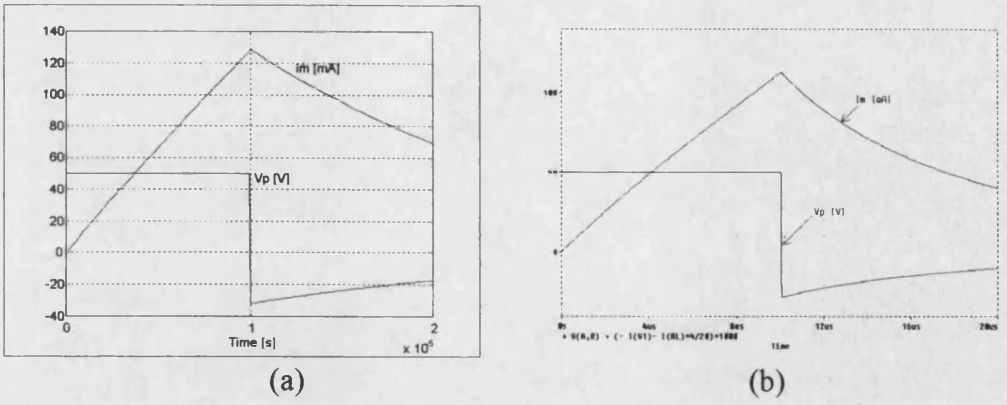
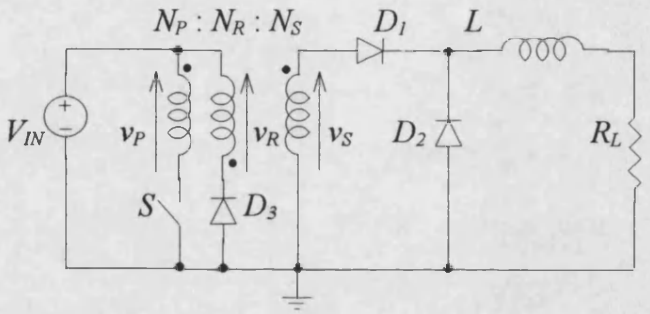


Fig. 13-4 The simulated primary voltage and magnetising current using a) MATLAB and b) PSPICE models



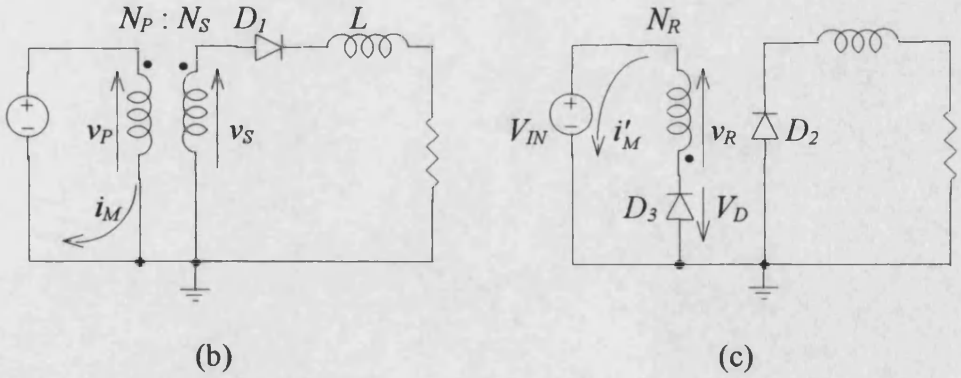


Fig. 13-5 a) Single-ended forward converter and the equivalent circuit in two cases: b) the switch is "on" and c) the switch is "off"

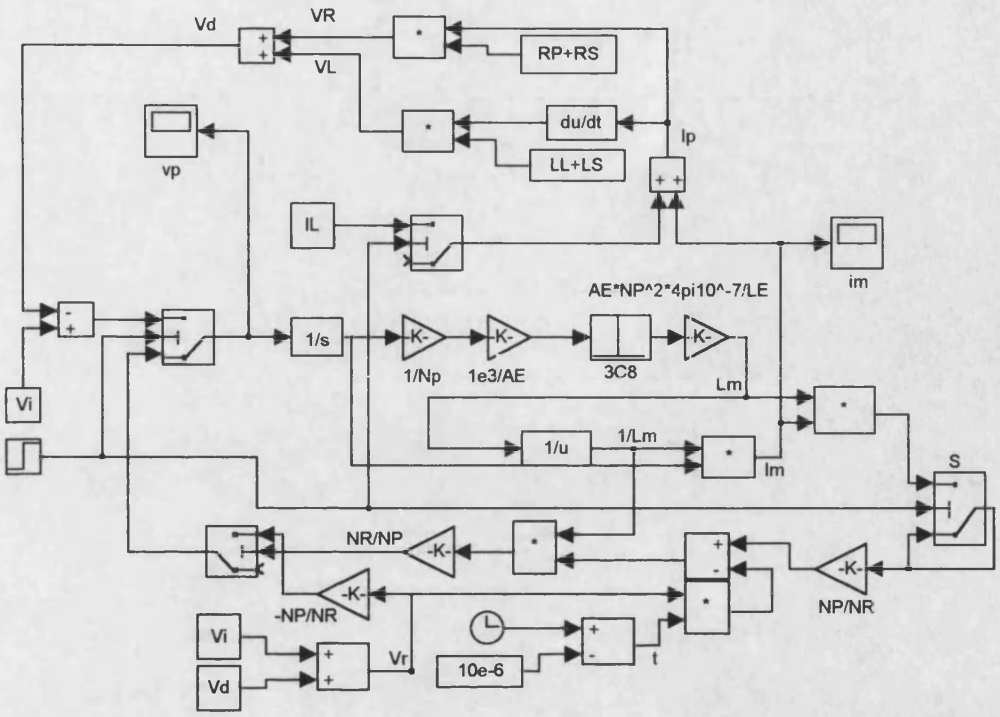
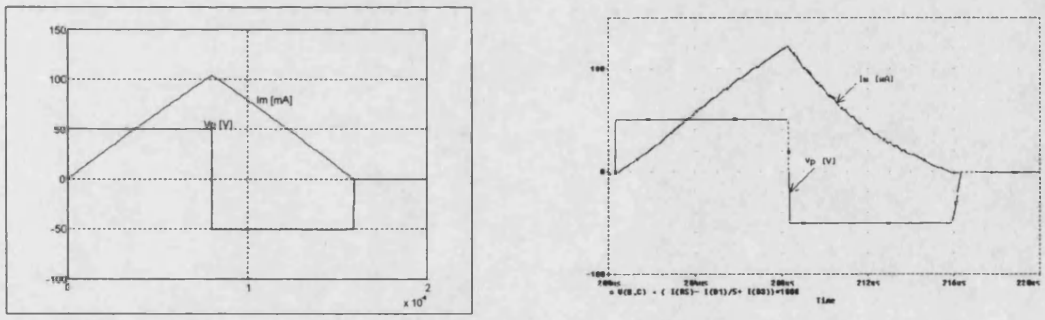
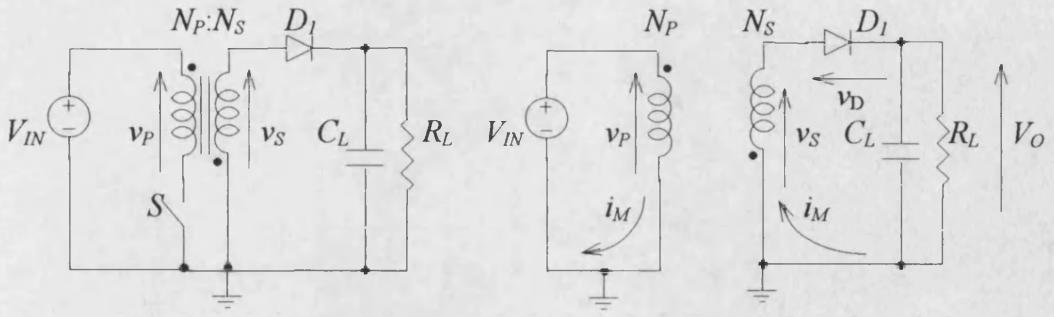


Fig. 13-6 MATLAB single-ended forward converter model



(a) (b)

Fig. 13-7 Simulated magnetising current and primary voltage using a) MATLAB and b) PSPICE models



(a) (b) (c)

Fig. 13-8 a) A flyback dc/dc converter and the equivalent circuit when b) the switch is "on" and c) the switch is "off"

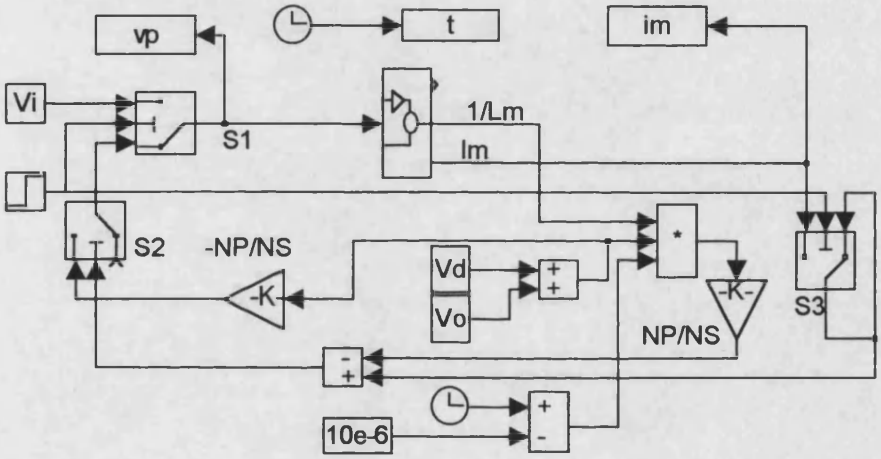
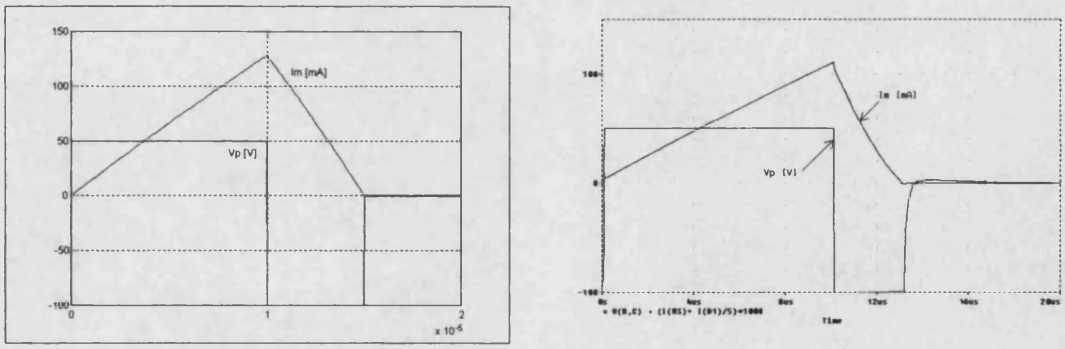


Fig. 13-9 MATLAB model for flyback converter



(a) (b)

Fig. 13-10 Simulated primary voltage and magnetising current for flyback converter using a) MATLAB and b) PSPICE models

THREE-PHASE TRANSFORMER MODELLING

14-1 INTRODUCTION

To model a three-phase transformer, a full understanding of the interaction between primary windings, on the one hand, and between primary and secondary windings, on the other, is required. To do this, it is necessary to determine the shape of the flux in each limb, since it defines secondary voltages and magnetising currents in each phase.

A number of different core geometries may be used in the construction of three-phase transformers, such as three-, four- or five-limb types, and any modelling procedure should ideally be usable with any core geometry.

The shell-type arrangement is simply constructed from three single-phase transformers with their cores laid end-to-end as shown in Fig. 14-1. However, it is possible to save the yokes of the middle transformer such that other yokes can be used as common magnetic paths, as shown in Fig. 14-2, thus reducing number of yokes from six to four. This results in appreciable saving in material, which leads to a reduction in transformer cost and volume saving.

In Fig. 14-2, the middle yokes are common to two magnetic paths, but the limbs do not take part of the sharing. However, it is possible, by rearranging the cores as shown in Fig. 14-3, to save more material.

Let us assume that a three-phase voltage source is applied to the three primary windings having the same number of turns wound on a core such that shown in Fig. 14-3. The resulting flux in each limb will be defined by the voltage applied to the winding on that limb. The flux waveforms will be 120° out of phase, as shown in

Fig. 14-4, and lag the voltage waveforms by 90°. The sum of the three flux waveforms is zero at any time, i.e.

$$\phi_1 + \phi_2 + \phi_3 = 0 \qquad (14\text{-}1)$$

This means that if the primary windings have the same number of turns, and the magnetic paths have the same reluctance, the sum of the three flux waveforms is always zero. Any core material carrying the sum of the flux waveforms, such as the centre limb shown in Fig. 14-3, can now be omitted without affecting the operation of the transformer, since zero flux is carried. Thus, each separate magnetic circuit uses the other two magnetic circuits, and the core will look like that shown in Fig. 14-5.

To make the construction of this core easier, the three remaining limbs are arranged in a straight line as shown in Fig. 14-6, and is called a core-type arrangement. This results in some lack of symmetry in the magnetic paths and, as a consequence, different magnetising currents, but in most cases this is not of a great importance [1].

14-2 THREE-PHASE TRANSFORMER OPERATION

In a three-limb three-phase transformer, as shown in Fig. 14-6, let us assume that a voltage is applied to the first primary only. If v_1 is a sinewave voltage having the following form:

$$v_1 = \hat{V} \sin \omega t \qquad (14\text{-}2)$$

then the flux in the first limb, assuming that all primary windings have the same number of turns, N, is given by:

$$\phi_1 = -\frac{1}{N}\int v_1 dt = -\frac{1}{N}\int \hat{V}\sin\omega t dt = \frac{\hat{V}}{N\omega}\cos\omega t \qquad (14\text{-}3)$$

If no voltage is applied on the other two windings, then, assuming that all magnetic paths have the same reluctance, half of ϕ_1 will flow in each limb and in the opposite direction such that:

$$\phi_2 = \phi_3 = -\frac{\phi_1}{2} = -\frac{\hat{V}}{2N\omega}\cos\omega t \qquad (14\text{-}4)$$

If, however, another sinewave voltage v_2 with a phase shift of θ_1 is applied to the centre winding, the flux in the centre leg is only determined by the second voltage v_2, and is given by:

$$\phi_2 = -\frac{1}{N}\int v_2 dt = -\frac{1}{N}\int \hat{V}\sin(\omega t - \theta_1)dt = \frac{\hat{V}}{N\omega}\cos(\omega t - \theta_1) \qquad (14\text{-}5)$$

At this stage, the flux in the left leg is defined by v_1, the flux in the centre leg is defined by v_2, and the flux in the right leg may be found from Eq. 14-1:

$$\phi_3 = -(\phi_1 + \phi_2) = -\frac{\hat{V}}{N\omega}\cos\omega t - \frac{\hat{V}}{N\omega}\cos(\omega t - \theta_1)$$

$$\phi_3 = -\frac{\hat{V}}{N\omega}[\cos\omega t + \cos(\omega t - \theta_1)] \qquad (14\text{-}6)$$

Since $\cos(A - B) = \cos A\cos B + \sin A\sin B$, Eq. (14-6) can be rewritten as:

$$\phi_3 = -\frac{\hat{V}}{N\omega}[\cos\omega t + \cos\omega t\cos\theta_1 + \sin\omega t\sin\theta_1] \qquad (14\text{-}7)$$

In three phase systems, θ_1=120°. Therefore, $\cos\theta_1 = -0.5$ and $\sin\theta_1 = 0.866$, which gives:

$$\phi_3 = -\frac{\hat{V}}{N\omega}(0.5\cos\omega t + 0.866\sin\omega t) \qquad (14\text{-}8)$$

This flux already exists without v_3 being applied to the right winding. If now a voltage v_3 with a phase shift of $\theta_2 = 240°$ is applied to the right winding, the flux in the right leg will be defined by v_3 such that:

$$\phi_3 = -\frac{1}{N}\int v_3 dt = -\frac{1}{N}\int \hat{V}\sin(\omega t - \theta_2)dt = \frac{\hat{V}}{N\omega}\cos(\omega t - \theta_2) \qquad (14\text{-}9)$$

which can be rewritten as:

$$\phi_3 = \frac{\hat{V}}{N\omega}(\cos\omega t\cos\theta_2 + \sin\omega t\sin\theta_2) \qquad (14\text{-}10)$$

But $\cos\theta_2 = \cos 240° = -0.5$, and $\sin\theta_2 = \sin 240° = -0.866$, hence:

$$\phi_3 = \frac{\hat{V}}{N\omega}(-0.5\cos\omega t - 0.866\sin\omega t)$$

$$\phi_3 = -\frac{\hat{V}}{N\omega}(0.5\cos\omega t + 0.866\sin\omega t) \qquad (14\text{-}11)$$

Comparing Eq's (14-8) and (14-11), which define the flux in the right leg before and after applying v_3, it can be noticed that they are identical. This means that the flux in the right leg, before applying v_3, is the same flux which should have been induced if v_3 was applied. In other words, a voltage v_3 was induced across the third primary even before v_3 was applied. This is why a three-phase voltages can be connected on a three-limb core and share the same magnetic paths.

PSPICE simulation has shown that if a flux already exists in a core due to a voltage applied to a winding, and another voltage is applied to another winding on the same core such that it produces the same flux which already exists in the core, the two

windings will share the same current which was flowing before applying the second voltage, i.e. each primary conducts half of the previous current.

From the above discussion, it is concluded that each limb works as a separate single-phase transformer with its own primary and secondary. But the feature of the three-phase transformer is that each of the individual single-phase transformers uses the other two limbs to complete its circuit, and there is no need for an extra limb. This of course is due to the 120° phase shift between the voltages, and hence the fluxes as have been seen. Thus appreciable transformer material and volume is saved, which means a reduction in cost and weight.

However, if the reluctances of the three magnetic paths are not equal, as in a core such that shown in Fig. 14-6, the sum of the three flux waveforms is not zero. In this case, the sum completes its magnetic path through the surrounding air and will not be linked to any other magnetic circuit. The next section briefly describes the effect of asymmetry in a three-limb three-phase core.

14-3 ASYMMETRY IN THREE-LIMB THREE-PHASE TRANSFORMERS

In three-phase three-limb transformers, each limb is concerned with one phase, and the magnetic circuit is completed through the other two phases in parallel. Since three-limb three-phase transformers, as that shown in Fig. 14-6, have an asymmetrical magnetic circuit, the magnetising currents in each phase are different. With this type of cores, the central phase has a magnetic circuit of lower reluctance than that of either of the outer phases. Therefore, its magnetising current is a few per cent less [2].

Generally, limbs are longer than yokes, and have a smaller cross-sectional area. This means that limbs have higher reluctance than yokes. Therefore, the yoke reluctance is only a small fraction of the total, so that the unbalance in magnetising current is small. Also, in transformers of normal design, the magnetising current is of the order

of 5% of the full-load current [2], and considerable variation in it may be made without affecting the performance of the transformer on load.

14-4 MATERIAL SAVING IN THREE-PHASE TRANSFORMERS

It is well known that a single three-phase transformer has a smaller size, and hence weight, than three single-phase transformers rated for the same *VA* capacity.
Flanagan [3] anticipated that a saving of (10-30)% of the total weight is possible, depending on the geometry of the core, but does not show how this saving can be calculated, and how it depends on the geometry. The following sections describe in details how saving can be calculated from the geometry of the core used for different core arrangements.

14-4-1 Material Saving in Three-Limb Core-Type Arrangements as Shown in Fig. 14-6

If a core such that shown in Fig. 14-7 is used for a single-phase transformer with a window area of $h_1 \cdot l_1$, and a core as shown in Fig. 14-8 is to be constructed to fit all three windings of the three single-phase transformers, then a saving in the surface of the three-phase core, and hence a saving in the size and weight, is gained as shown in the shaded parts in Fig. 14-7. Also, some modifications of one of the three sections in Fig. 14-7 is required to fit two adjacent windings, as shown by the addition of the shaded parts in Fig. 14-8. Therefore the net saving in material:

$$S_1 = 3h_2 w - 2l_1 w$$

$$S_1 = w(3h_2 - 2l_1) \qquad (14\text{-}12)$$

where $h_2 w$ is the saving in each single-phase core, and $2l_1 w$ is the material needed to fit the two adjacent windings. It is assumed that w and cross-sectional area are constant along the whole magnetic length of the core. From Fig. 14-7, the total surface needed for the three single-phase transformers is:

$$S_2 = 3(2h_2 w + 2l_1 w) = 6w(h_2 + l_1) \tag{14-13}$$

The normalised saving is:

$$S_N = \frac{S_1}{S_2} = \frac{w(3h_2 - 2l_1)}{6w(h_2 + l_1)} = \frac{3h_2 - 2l_1}{6(h_2 + l_1)} \tag{14-14}$$

which shows that saving in material depends on l_1, the window width, and h_2, the height of the core.

Examples of material saving in three-phase cores

1. A core as shown in Fig. 14-9, where $h_2 = 5$ cm, $l_1 = 6$ cm:

$$S_N = \frac{3 \times 5 - 2 \times 6}{6(5+6)} \approx 4.5\%$$

2. Same as in Fig. 14-9 with h_2 and l_2 being interchanged to give $h_2 = 8$ cm, $l_1 = 3$ cm:

$$S_N = \frac{3 \times 8 - 2 \times 3}{6(8+3)} \approx 27.3\%$$

3. A core as shown in Fig. 14-7, where $h_2 = 5$ cm, $l_1 = 12$ cm:

$$S_N = \frac{3 \times 5 - 2 \times 2}{6(5+2)} \approx 26.2\%$$

4. A square core such as that shown in Fig. 14-10, with $w = 0.12h_2$, a practical case:

$$S_N = \frac{3h_2 - 2(h_2 - 2w)}{6[h_2 + (h_2 - 2w)]} = \frac{3h_2 - 2(h_2 - 0.4h_2)}{6(h_2 + h_2 - 0.4h_2)} \approx 18.8\%$$

This saving is true for any square-windowed core, with $w = 0.12h_2$. If h_2 is described relative to l_1, i.e. $k = h_2/l_1$ where k is constant, a general formula for the normalised material saving is obtained:

$$S_N = \frac{3h_2 - 2l_1}{6(h_2 + l_1)} = \frac{3k - 2}{6(k + 1)} \quad \text{, where } k \geq 2/3 \qquad (14\text{-}15)$$

Fig. 14-11 shows the normalised material saving as a function of k, from which it can be noticed that as k increases, i.e. l_1 decreases or h_2 increases, the saving increases. For $k = 2/3$, i.e. $l_1 = 1.5h_2$, the saving is zero. Practical transformer cores must have a k value at or above 2/3. Therefore, to save weight and size, k must be higher than 2/3, i.e. l_1 should be less than $1.5h_2$. From Eq. (14-15) it is seen that the maximum theoretical saving is 50%, which occurs as $k \to \infty$. Of course, very large k values are not practical; therefore, a saving approaching 50% is not achievable. Normalised saving values of the previous four examples are marked on Fig. 14-11 by their example numbers. App. (14-1) lists a MATLAB program used to draw Fig. 14-11.

14-4-2 Material Saving in Three-Limb Core-Type Arrangements as Shown in Fig. 14-5

If a core, as shown in Fig. 14-5, is to be constructed from the same three single-phase cores shown in Fig. 14-7, material saving is calculated by first assuming a square cross-sectional area, w^2, for each limb. The saved parts are identified and shown by the shaded areas in Fig. 14-7:

$$S_S = 3h_2 w \qquad (14\text{-}16)$$

If the same window width (l_1 in Fig. 14-7) is used, the windings cross each other. To accommodate for this, l_1 should be increased such that the three windings just touch

each other as shown in Fig. 14-12. It is assumed in Fig. 14-12 that the windings form cylinders with the central axis of each one lying on the central axis of the corresponding limb. It can be seen from Fig. 14-12 that a distance a is required to accommodate for the three windings, where a may be found as follows:

$$b\cos 30 = r \Rightarrow b = \frac{r}{\cos 30} = \frac{2r}{\sqrt{3}} \tag{14-17}$$

$$c = \frac{w}{2}\tan 30 = 0.289w \tag{14-18}$$

$$a = b - r - c = \frac{2r}{\sqrt{3}} - r - 0.289w = 0.155r - 0.289w$$

$$a = 0.155(l_1 + w/2) - 0.289w = 0.155l_1 - 0.212w \tag{14-19}$$

where r is the radius of the winding, and b is the distance from the axis of each limb to the axis of the three-phase core. For each phase, the required area is aw. The total required area including the centre part, and for the two sides of the core:

$$S_R = 2[3(0.155l_1 - 0.212w)w + w^2 \sin 60/2]$$

$$S_R = 0.93l_1w - 1.272w^2 + 0.866w^2 = w(0.93l_1 - 0.406w) \tag{14-20}$$

The net surface saving:

$$S_1 = S_S - S_R = 3h_2w - w(0.93l_1 - 0.406w) \tag{14-21}$$

The normalised material saving:

$$S_N = \frac{S_1}{S_2} = \frac{3h_2w - w(0.93l_1 - 0.406w)}{6w(h_2 + l_1)} \tag{14-22}$$

If h_2 and w are described relative to l_1, i.e.

$$k = \frac{h_2}{l_1},\ c = \frac{w}{l_1} \tag{14-23}$$

then Eq. (14-22) may be written as:

$$S_N = \frac{3k - (0.93 - 0.406c)}{6(k+1)} \tag{14-24}$$

Fig. 14-13 shows how S_N varies with k for different values of c. Superimposed on Fig. 14-13 is the curve of Fig. 14-11, where it is clearly seen that saving of the core such that shown in Fig. 14-5 is always higher than that shown in Fig. 14-6 irrespective of c values. App. (14-2) lists a MATLAB program used to draw Fig. 14-13.

14-5 A PSPICE THREE-PHASE TRANSFORMER MODEL

A method of modelling a three-limb three-phase transformer in PSPICE is shown in Fig. 14-15. The corresponding netlist is given in App. (14-3). The model is based on the analysis introduced in Sec. (14-2). It is assumed that the three magnetic circuits of the core have the same reluctance, i.e. the core is as shown in Fig. 14-5.

14-5-1 Model Description

The model employs three separate cores as sub-circuits. Each sub-circuit represents one limb of the three-limb core, and are named limb1, limb2 and limb3 in Fig. 14-15. Each limb has its own primary and secondary windings, and another winding which is included to represent additional mutual inductance effects between transformer phases. Thus, L_{11}, L_{12} and L_{13} represent primary windings of the three limbs; L_{21}, L_{22} and L_{23} represent secondary windings; L_{31}, L_{32} and L_{33} represent the mutual inductance effects.

The switch S_2 and the voltage source V_2 work as follows:

As presented in Sec. (12-2-2), PSPICE always assumes that a virgin core is started with, i.e. the flux always starts from zero irrespective of the initial value of the

voltage that induces this flux. The lack of an ability to set initial values of core flux, introduces an initial flux transient which may take a long time to decay to zero. Therefore, a procedure has been developed to quickly establish steady-state flux conditions, which will now be briefly described:

The first phase voltage applied between points 1 and 2 in Fig. 14-15 is delayed such that it starts at a peak value; the second phase voltage applied between points 3 and 4 is not applied to the second primary, L_{12}, until a peak (positive or negative) is reached. This is done using a switch, S_2, which is turned "on" at a voltage peak. The switch then stays "on" for the rest of the simulation . The switch may be controlled by a pulsed voltage source model "Vpulse" or a piece-wise-linear voltage source "Vpwl", available in PSPICE. In Fig. 14-15, a piece-wise-linear voltage source, V_2, is used to control the switch.

The times between brackets under the voltage source, show the time at which the voltage source switches from zero to 0.1 V to turn the switch "on". This time is calculated based on the operating frequency. Hence, this time should be changed if another frequency is assumed. Because the switch should be turned "on" quickly (ideally in zero time), non-convergence problems occurred. To solve this, the switch was allowed to turn "on" during the μs time-range given in brackets. This time range was calculated such that a voltage peak lies in the middle of this range. If the time range is too large, there will be a flux shift from zero which could be positive or negative. On the other hand, if the time range is too small, a non-convergence problem is invariably occurs. A compromise must be made to obtain workable time range. Also to help solve non-convergence problems, a new switch model was created which is turned "on" at 0.1 V instead of 1 V assumed in PSPICE switch model. This reduction in voltage threshold, reduces the dV/dt of the command voltage applied on the switch terminals, and thus helps eliminate non-convergence problems.

The switch S_4 and the voltage source V_5 work exactly as described for S_2 and V_2, but apply for the third winding between points 5 and 6. Fig. 14-16 shows phase voltages and flux waveforms for the three limbs. The times at which all switches are turned "on" are also shown.

The voltage source, E_1, works as follows: The flux in the first limb is defined by the first phase voltage. As described earlier in Sec. (12-2-2), even if the phase voltage, V_1, is not applied to the first primary, the flux in the first leg exists due to the other two phase voltages. To include this effect, a voltage source, E_1, which equals the sum of the other two voltages, is added. This voltage is applied in such a direction that it produces an opposite flux in the first limb as suggested by Eq. (14-1), where:

$$\phi_1 = -(\phi_2 + \phi_3) \tag{14-25}$$

The same argument applies for the voltage sources E_3 and E_5. Switches S_1, S_3 and S_5 are used to introduce the above-mentioned effects after the flux in the three limbs are established. All these switches are controlled by the same command generated by the voltage source V_4. During simulation, it has been noticed that it is better to start the effect of E_1, E_3 and E_5 when the flux in one limb is zero. Therefore, the time range between brackets under V_4 is calculated such that the flux in the first limb is zero (see Fig. 14-16).

The current source G_1 works as follows: Because two coils L_{11} and L_{31} that work as primary windings with their associated voltage sources (the phase voltage V_1 and the voltage E_1) exist, any current drawn from the secondary L_{21} will be drawn from L_{11} and L_{31} equally. However, in practice, the current drawn from the first secondary is drawn only from the first primary. Therefore, to compensate for the current drawn from E_1, another current source, G_1, should be added ; This current equals the current flows in E_1, which is sensed by V_{S1}. The same argument is applied for G_2, G_3, V_{S3} and V_{S6}.

14-5-2 Model Testing

To test the validity of the model, a connection between the three-phase source and transformer neutral points, as shown in Fig. 14-14, will initially be used to represent a four wire, star/star connection. The waveforms obtained from simulation were compared with practical waveforms given in [4]. A supply frequency of 100 kHz,

voltage amplitude of 100 V, and a core-type ETD59_N67 will be assumed in this simulation.

The neutral current, which is the sum of the three phase currents, $i_{An}+i_{Bn}+i_{Cn}$,, where n denotes harmonic number, is zero for positive [1,4,7,...,(3m+1)] and negative [2,5,8,...,(3m-1)] sequence components, and three times i_{An} for zero [3,6,9,...,(3m+3)] sequence components.

Fig. 14-17a and b show the spectrum of the neutral and phase currents for the circuit shown in Fig. 14-14, while Fig. 14-17c shows the neutral and phase currents with time. From the figure, it is seen that the neutral current contains no positive and negative components, and has mainly the third harmonic (300 kHz) with an amplitude of 33 mA, which is three times the phase current ($\approx$ 11 mA at 300 kHz). Also seen is the ninth harmonic (900 kHz) with an amplitude of 500 μA which is three times the phase current ($\approx$ 167 μA at 900 kHz).

The phase current should be identical to the one in single-phase transformers. This current contains a large third harmonic, and small values of other odd harmonics. The third harmonic is 11 mA compared with the fundamental, 93 mA, which is 12%. While Reference [4] says that this ratio should be (30-50)%, Reference [5] says that, when the flux is sinusoidal, this ratio should be (13-40)% of the fundamental, depending on the flux density, B; it increases as B increases.

Fig. 14-18 is the same as Fig. 14-17, but the input voltage is increased from 100 V to 200 V and the flux density is doubled. From this figure, the ratio of the third harmonic of the phase current, (25.8 mA), to the fundamental, (157.2 mA), is 16.4% compared to 12% when the voltage was 100 V. Other harmonics are also increased, and the ninth harmonic (5.8 mA) is now 7.5% of the third harmonic (77.5 mA). This ratio was (0.5/32.8)=1.5% when the voltage was 100 V. The third harmonic of the neutral current is three times the phase current. It is clear that the phase currents only contain odd harmonics, and the neutral current contains only triplen harmonics as should be the case in a four-wire system.

The difference between two phase harmonic currents, e.g. i_{An}-i_{Bn} should be equal to 0, $\sqrt{3}\, i_{An}\, e^{\,j30}$, $\sqrt{3}\, i_{An}\, e^{\,j-30}$ for zero, positive and negative sequence components, respectively. Fig. 14-19 shows this difference together with i_{An} . From the figure it can be seen that the amplitude of the zero sequence components of i_{An}-i_{Bn} obtained by

simulation is zero. On the other hand, Table (14-1) which was obtained from simulation, shows that for negative and positive sequence components (1, 5, 7), the amplitude is equal to $\sqrt{3}\, i_{An}$.

harmonic number	i_{An}-i_{Bn} (mA)	i_{An} (mA)
1	161	93
5	6.3	3.64
7	1.74	1

Table (14-1) Transformer magnetising-current frequency-component values extracted from three-phase PSPICE transformer model

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1. F. C. Connelly, "Transformers: their principles and design for light electrical engineers", Sir Isaac Pitman & Sons Ltd., London, 1965.
2. M.G. Say, "The performance and design of alternating current machines", Pitman Paperbacks, Bath, 1958.
3. W.M. Flanagan, "Hand book of transformer applications", McGraw Hill, New York, 1986.
4. Y. Baghzouz and X.D.Gong, "Analysis of three-phase transformer no-load characteristics", IEEE transactions on power systems, Vol. 10, No. 1, Feb. 1995, pp. 18-26.
5. M. Kostenko and L. Piotrovsky, "Electrical Machines", Part one, Peace Publishers, Moscow.

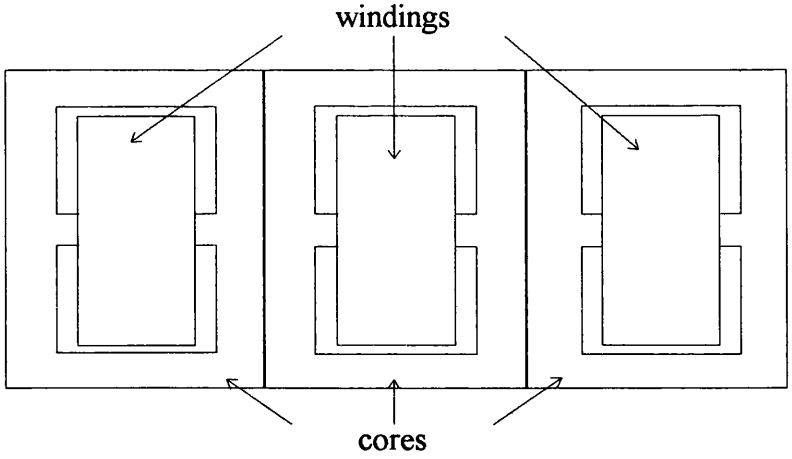


Fig. 14-1 Shell-type arrangement showing complete three single-phase transformers

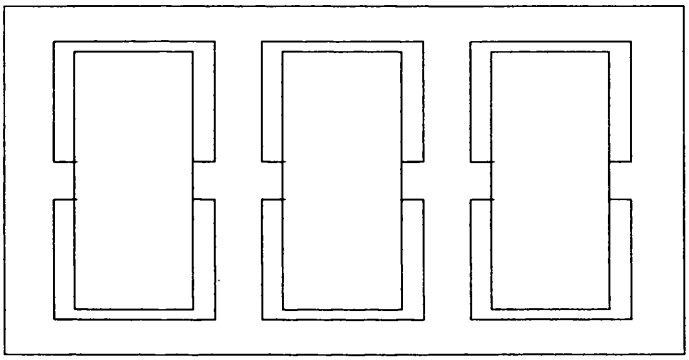


Fig. 14-2 Three-phase shell-type arrangement showing two yokes being removed

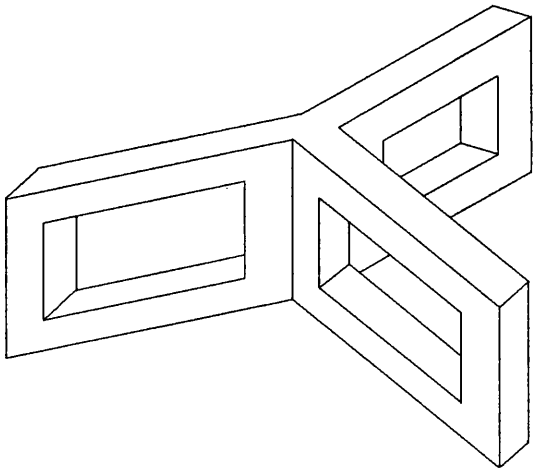


Fig. 14-3 Three core-type single-phase transformers as an introduction to show limb sharing

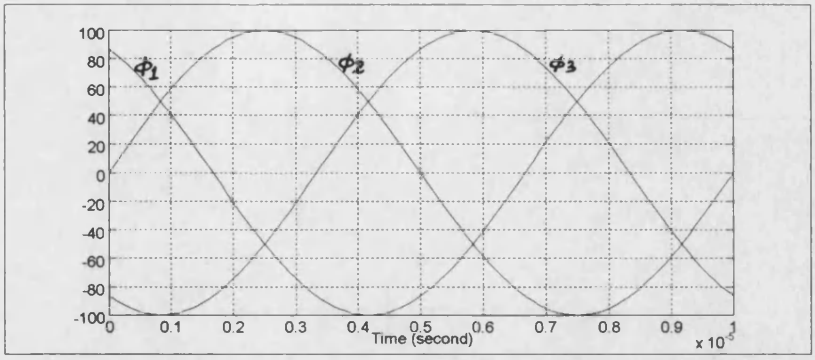


Fig. 14-4 Flux waveforms in a three-phase system

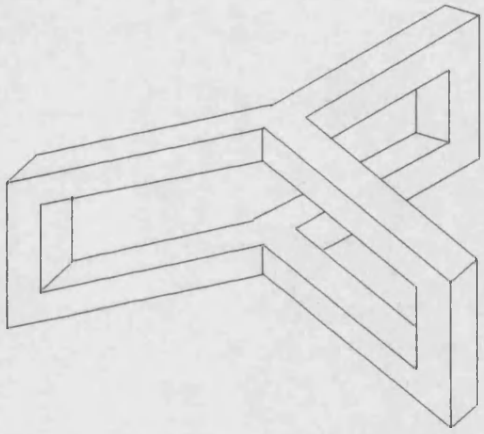


Fig. 14-5 Three-limb core-type arrangement showing central limb removed

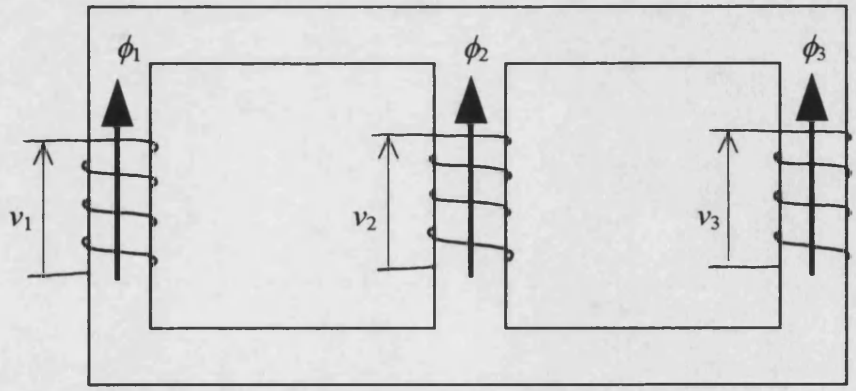


Fig. 14-6 A practical three-limb three-phase core-type arrangement

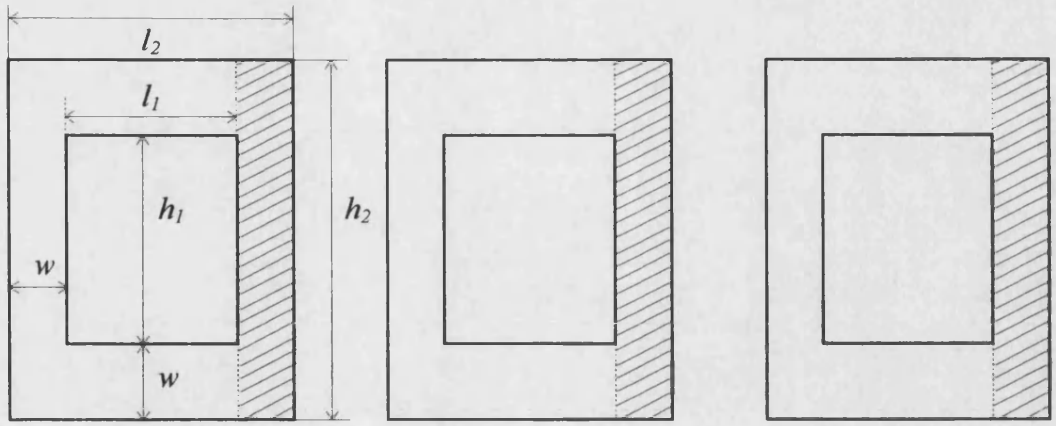


Fig. 14-7 Three single-phase transformer cores showing sections removed as a first step in constructing a three-phase transformer core

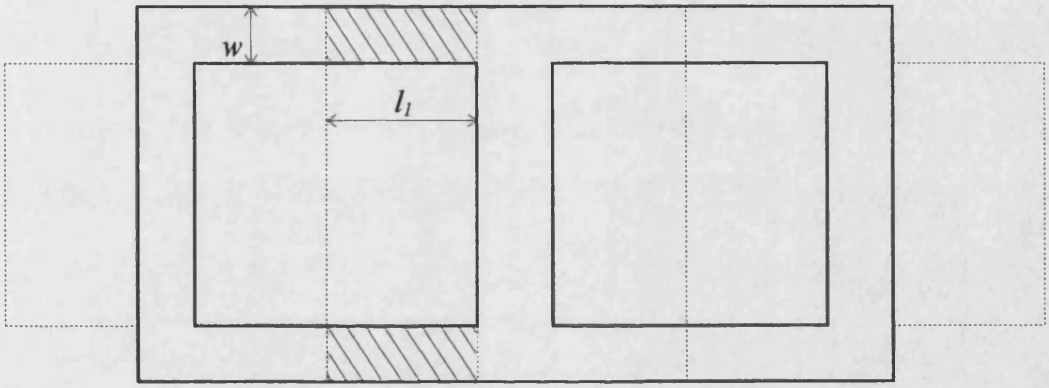


Fig. 14-8 Three-phase transformer core developed from three single-phase cores, showing added section to accommodate for the centre-limb winding

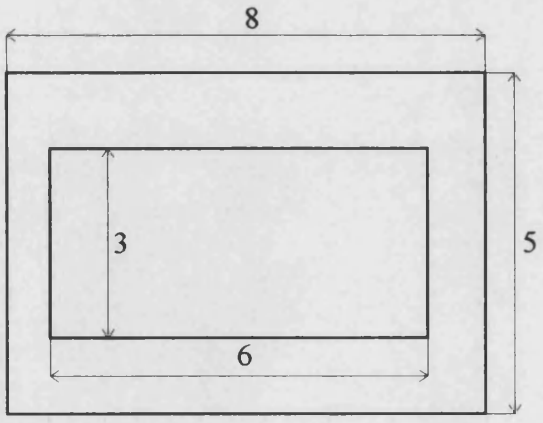


Fig. 14-9 A core used in example 1

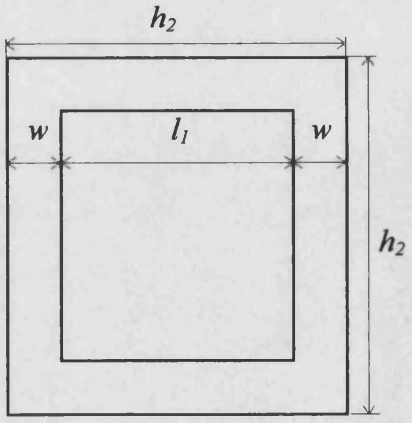


Fig. 14-10 A core used in example 4

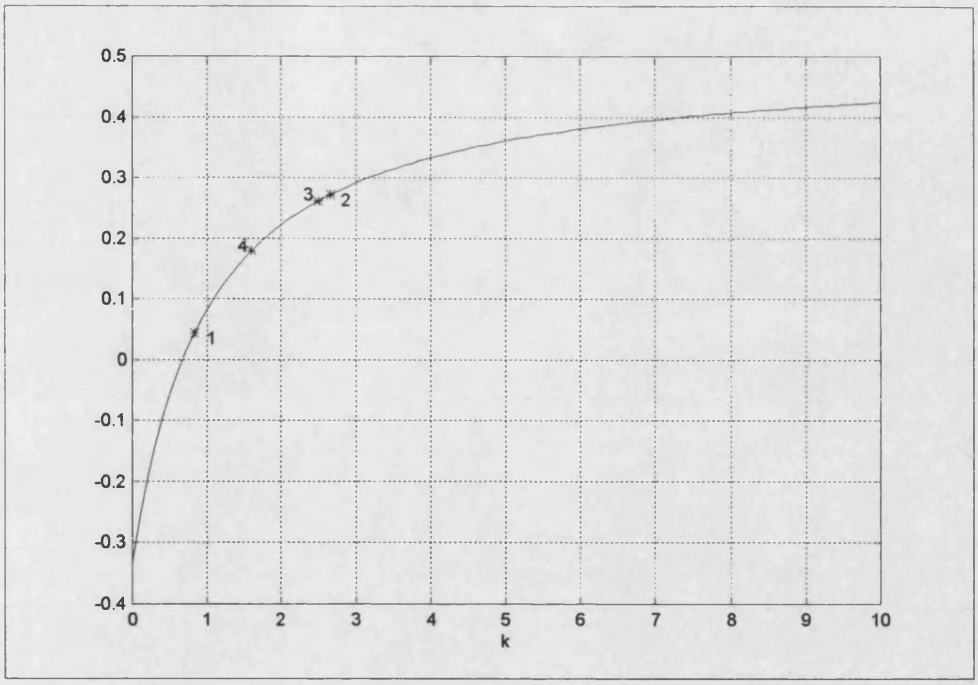


Fig. 14-11 Normalised material saving for practical three-limb core-type arrangements as a function of k [see App. (14-1) for MATLAB file]

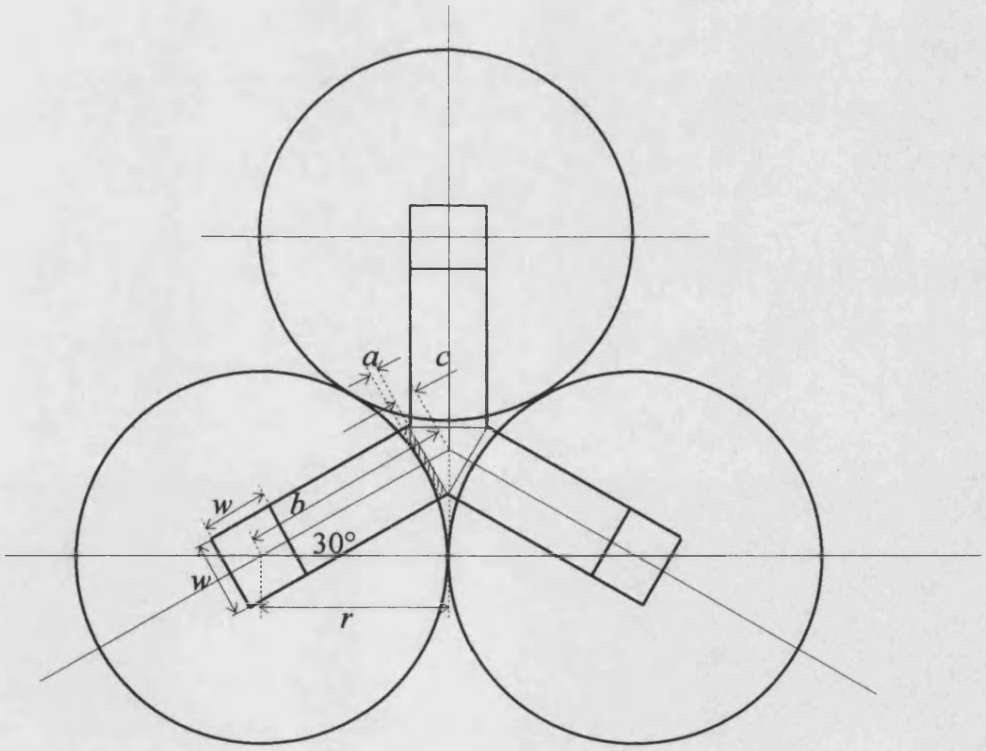


Fig. 14-12 Calculating the distance a required to accommodate for the three windings

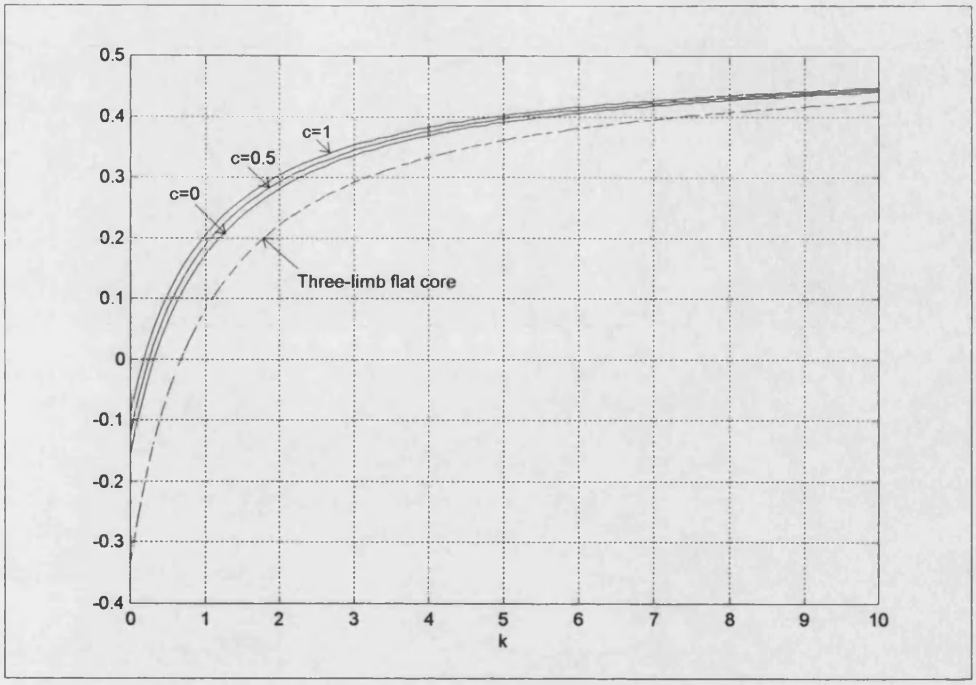


Fig. 14-13 Normalised material saving for the core of Fig. 14-5, as a function of k [see App. (14-2) for MATLAB file]

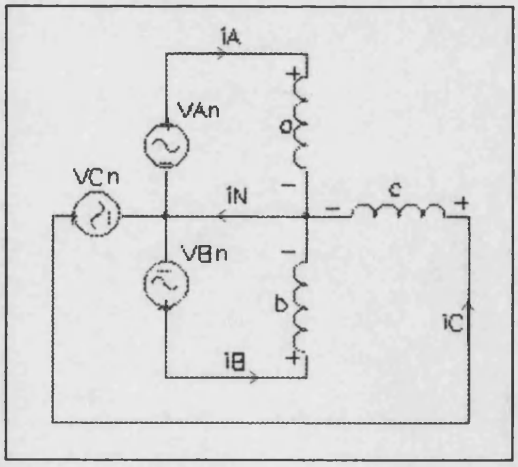


Fig. 14-14 A circuit used to test the three-phase transformer

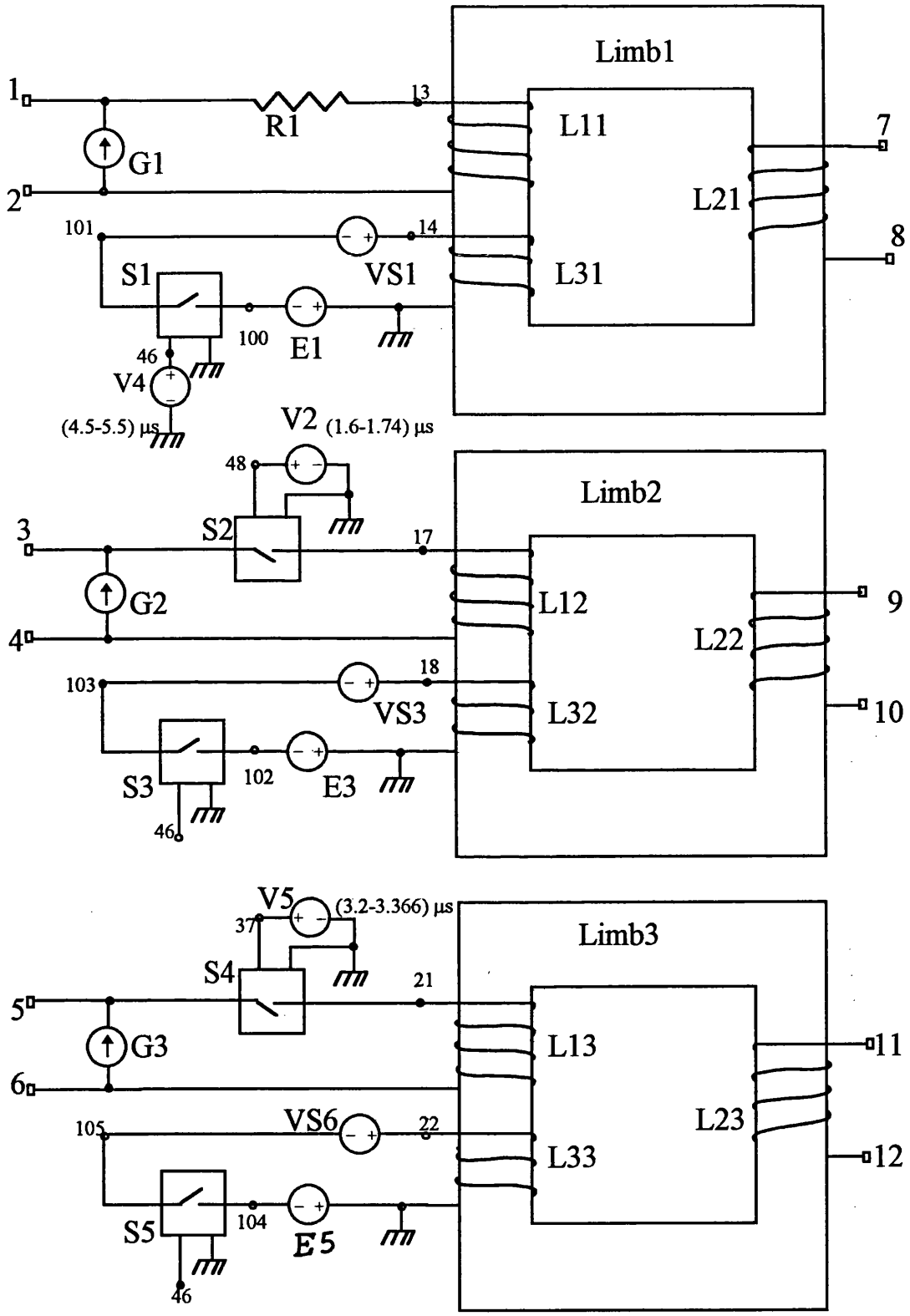


Fig. 14-15 A PSPICE three-limb three-phase transformer model

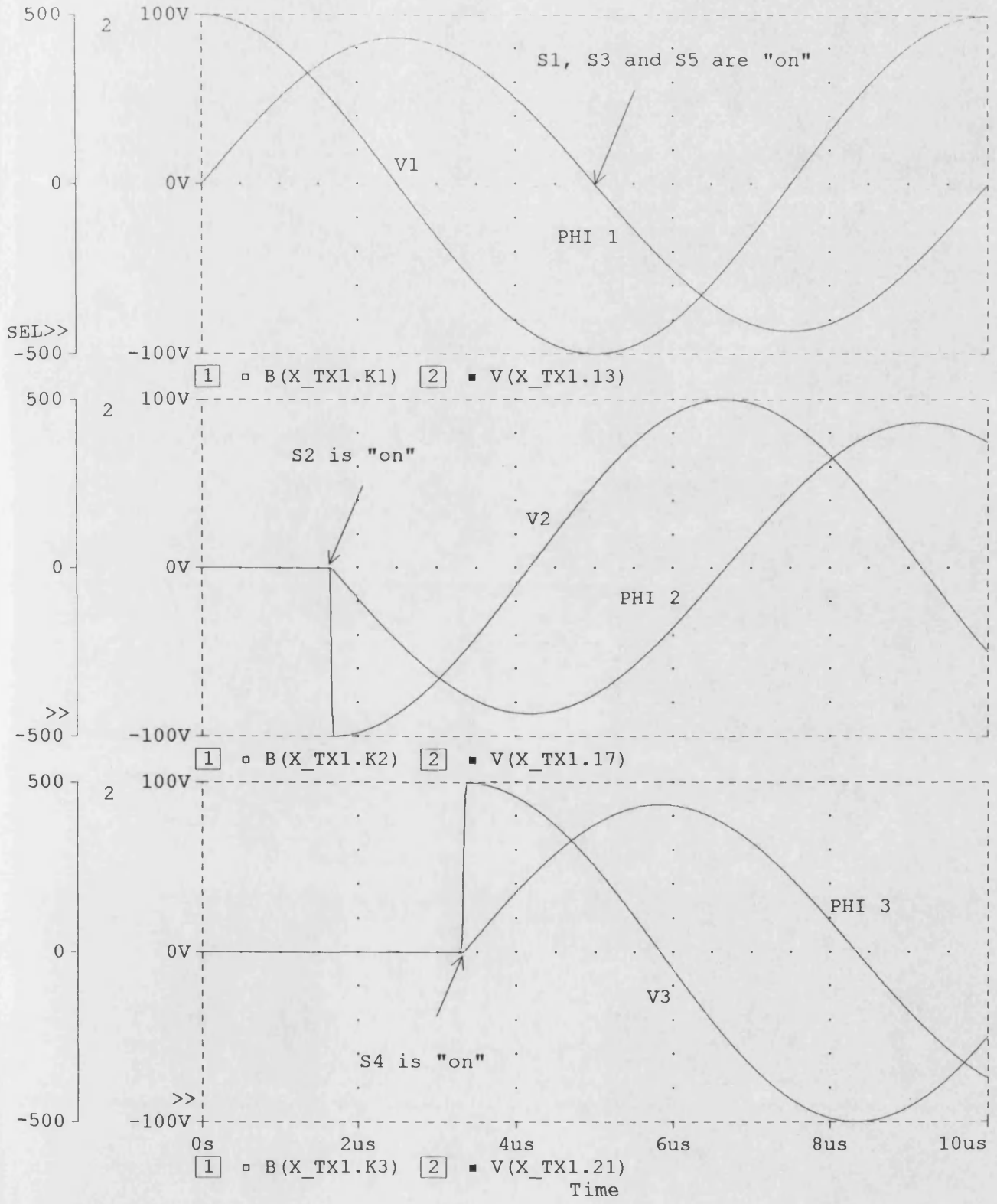
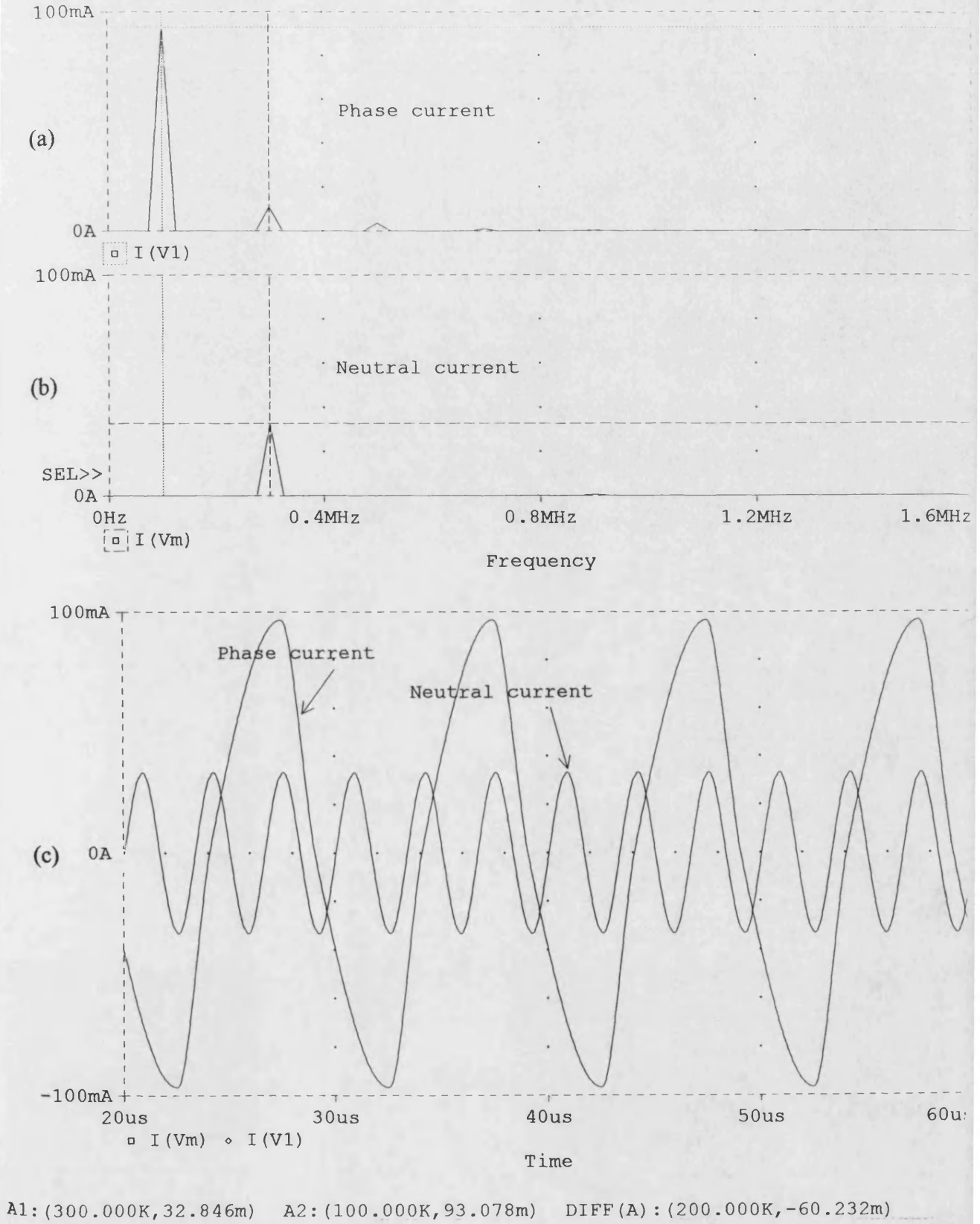


Fig. 14-16 Voltage and flux waveforms in a three-limb three-phase transformer



A1:(300.000K,32.846m) A2:(100.000K,93.078m) DIFF(A):(200.000K,-60.232m)

Fig. 14-17 (a) The spectrum of a phase current, (b) the spectrum of the neutral current and (c) the neutral and phase currents with time, when the amplitude is 100 V

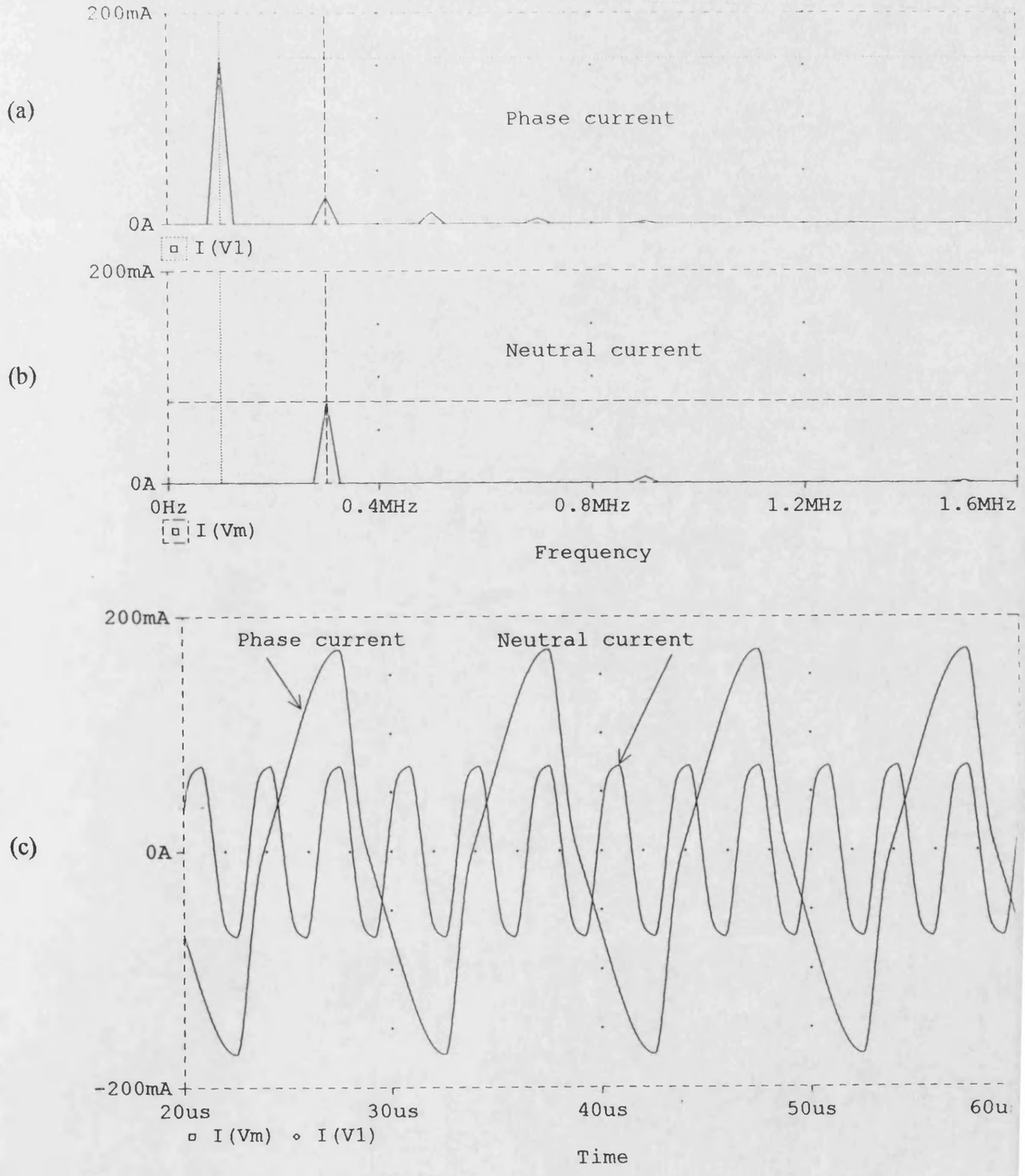


Fig. 14-18 (a) The spectrum of a phase current, (b) the spectrum of the neutral current and (c) the neutral and phase currents with time, when the amplitude is 200 V

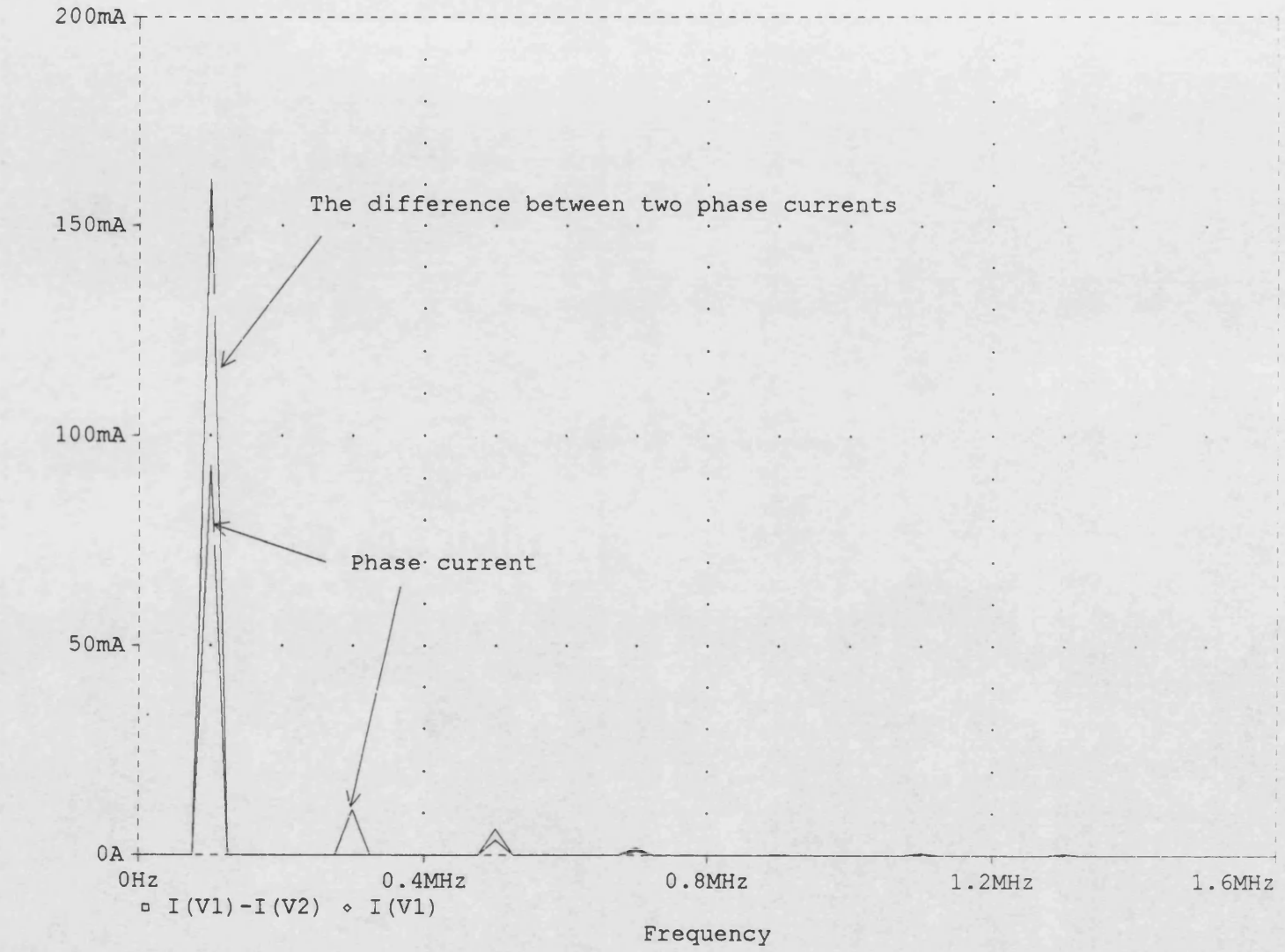


Fig. 14-19 The difference between two phase currents, and one phase current

THERMAL MODELLING

15-1 INTRODUCTION

Power loss in semiconductors is dissipated as heat which transfers away to the surrounding air to keep the junction temperature below a certain safe value.
The fact that the reliability of semiconductors reduces as temperature rises, calls for accurate modelling of junction and case temperature, which, together with electrical simulation, determines the design of the whole system.
The equation that relates power dissipation, P, to temperature rise, T, and thermal resistance, R_θ, is given by :

$$P = \frac{T_2 - T_1}{R_\theta} \qquad (15\text{-}1)$$

where P is the power dissipation, T_2 and T_1 are the temperature on both sides of the thermal system, and R_θ is the thermal resistance, as shown in Fig. 15-1. Eq. (15-1) resembles Ohm's law:

$$I = \frac{V_2 - V_1}{R}$$

where V_2 and V_1 are the voltage difference across the resistance, R. Therefore, a thermal system can be represented by an electrical circuit analogue, as shown in Fig. 15-2. The dissipated power is analogous to current, the thermal resistance is

analogous to resistance, and the temperature is analogous to voltage difference in an electrical system.

If the power dissipated in a thermal system is pulsed, as is frequently the case in most power electronics applications, then the temperature only increases during the pulse and decreases between pulses. The masses and material specific heat capacities of the pieces of material making up power semiconductor devices, determine the level of temperature ripple obtained during pulsed operation. This effect may be represented in the circuit analogue by a capacitance across the thermal resistance as shown in Fig. 15-3, and is called thermal capacitance, C_θ. A thermal system with a higher thermal capacitance can absorb more heat for the same temperature rise than a system with a lower thermal capacity, just as a higher electrical capacitance accepts more charge for the same voltage rise than a lower capacitance. Thermal capacitance is given by:

$$C_\theta = M \cdot c \text{ [J/K]}$$

where M is the mass [g], and c is the specific heat [J/gK]. The thermal resistance and capacitance together constitute thermal impedance, Z_θ.

Therefore, for Fig. 15-3 we can write:

$$p = p_C + p_R \tag{15-2}$$

$$p_C = C_\theta \frac{dT}{dt}, \qquad p_R = \frac{T}{R_\theta} \tag{15-3}$$

where T is measured relative to some reference temperature, say $T_{AMBIENT}$. From Eq's (15-2), (15-3) we can write:

$$p = C_\theta \frac{dT}{dt} + \frac{T}{R_\theta} \tag{15-4}$$

Solving for T in Eq. (15-4) gives :

$$T = pR_\theta(1 - e^{-t/\tau_\theta}) \tag{15-5}$$

where $\tau_\theta = R_\theta C_\theta$.

For two thermal components in series, the temperature rise is given by:

$$T = pR_\theta(1 - \frac{R_{\theta 1}}{R_\theta} e^{-t/\tau_{\theta 1}} - \frac{R_{\theta 2}}{R_\theta} e^{-t/\tau_{\theta 2}}) \tag{15-6}$$

where $R_\theta = R_{\theta 1} + R_{\theta 2}$, $\tau_{\theta 1} = R_{\theta 1} C_{\theta 1}$ and $\tau_{\theta 2} = R_{\theta 2} C_{\theta 2}$. Thermal impedance calculations for two and three thermal components in series are available, and the same, of course, is applied on systems having more than three components. So, with a thermal system having n components, the following formula can be used to describe the normalised thermal impedance $Z_{\theta n}(t)$:

$$z_{\theta n}(t) = \frac{z_\theta(t)}{R_\theta} = 1 - \frac{R_{\theta 1}}{R_\theta} e^{-t/\tau_{\theta 1}} - \frac{R_{\theta 2}}{R_\theta} e^{-t/\tau_{\theta 2}} - \ldots - \frac{R_{\theta n}}{R_\theta} e^{-t/\tau_{\theta n}} \tag{15-7}$$

where $R_\theta = R_{\theta 1} + R_{\theta 2} + \ldots + R_{\theta n}$, and $\tau_{\theta i} = R_{\theta i} C_{\theta i}$.

The physical interpretation of Eq. (15-7) is that at the beginning of the power dissipation, i.e. at $t = 0$, there is no temperature difference between the two sides of the thermal system, since the thermal capacitance tries to absorb this heat. As the time passes, the capacitance has absorbed some heat and the temperature begins to increase. After long time, say five times the maximum thermal time-constant, the temperature rise will be $p \cdot R_\theta$, and any power dissipated from the source will be dissipated by the thermal system to the surrounding air. The temperature then settles, and there will be little effect due to the capacitance, which only delays the temperature rise for some time depending on its value.

To model the temperature rise in an electrical system, it is essential to model its thermal properties, i.e. the thermal impedance of the system. The next section describes in details how the thermal impedance curve of semiconductors can be modelled, and how thermal capacitances and resistances can be calculated from the curve given in the data sheet.

15-2 THERMAL IMPEDANCE MODELLING OF SEMICONDUCTORS

Power semiconductor devices comprise several pieces of different materials with different thermal properties. The characteristics of these are not given in data sheets, but device manufacturers instead give thermal impedance curves to allow some quantification of their combined effect. Each thermal impedance curve can be simulated by an $R_\theta C_\theta$ network as shown in Fig. 15-4 [1-3]. The number of branches or complexity of the $R_\theta C_\theta$ network depends on the nature of the given thermal impedance curve; the more stages required for a piece-wise approximation to the thermal impedance graph or logarithmic axis, the more network branches, or $R_\theta C_\theta$ time-constants, are required to acceptably model the curve in a similar way to representing a complex response using a bode plot.

For instance, Fig. 15-5 shows the thermal curve for IRFP450 MOSFET [4]. Fig. 15-6 shows how this curve can be modelled using Eq. (15-7) with four network branches. Another curve as shown in Fig. 15-7 can be obtained using five network branches, where we notice a better fit at small pulse width values (below 10^{-3} s). Parameters from Fig. 15-7 were used as initial values for curve fitting in EASYPLOT curve-fitting software, where a third curve was obtained as shown in Fig. 15-8, which is described by the following equation:

$$z_{\theta n}(t) = 1 - ae^{-t/b} - ce^{-t/d} - fe^{-t/g} - he^{-t/k} - le^{-t/m} \qquad (15\text{-}8)$$

where

a =.0083, $b = 8.6149 \cdot 10^{-6}$, c =.0477, $d = 271 \cdot 10^{-6}$, f =.4446, $g = 56 \cdot 10^{-3}$, h =.0783, $k = 3.1 \cdot 10^{-3}$, l =.4215, m =.336.

The original curve was plotted using 21 data points from Fig. 15-5 at multiples of 10^{-5}, $2 \cdot 10^{-5}$, $3 \cdot 10^{-5}$, and $6 \cdot 10^{-5}$. The model was simulated in PSPICE at different duty cycles and showed a good agreement with the curve given in the data sheet [4].

A thermal model for MUR8100E fast recovery diode, was also produced and is shown in App. (15-1). A general procedure for finding an equivalent circuit model for any thermal impedance graph is also given in App. (15-2).

15-3 POWER DISSIPATION MODELLING

15-3-1 Introduction

When designing power electronics circuits, such as switching dc/dc converters, temperature estimation of power components, such as power switches and diodes, is an important part of the design since operating power semiconductors at excessive junction temperatures results in rapid device failure, and operating them at too low a temperature will result in excessive product cost. Therefore, it is necessary to be able to predict the case, and even the junction temperature before building the circuit, and buying circuit components. This facilitates sizing heat sinks and/or modifying circuit design if the temperature of some components is found to lie outside the safety margins.

15-3-2 Power Dissipation Calculations

If power semiconductors are operated in the switched-mode, as it is the case in most power electronic applications, total power loss comprises two components:

1. Conduction losses: If diodes and bipolar transistors are used, conduction losses can be calculated as $P_{COND}=V_O I_{AV} + I^2_{rms} r$, where V_o is the current-independent device voltage drop, I_{AV} is the average value of the conducted current waveform, and $I^2_{rms} r$ represents Ohmic voltage drop loss. If MOSFET's are used , conduction loss is calculated using $P=R_{ON} I^2_{rms}$, where R_{ON} is the "on" resistance of the MOSFET which is a variable parameter with current, and I_{rms} is the rms value of the conducted current waveform.

2. Switching losses: This component becomes a very significant term at high frequencies, since it is proportional to the operating frequency, $P_{SW} = f_{SW}(W_{ON} + W_{OFF})$. Switching energies W_{ON} and W_{OFF} are dependent on the speed at which the devices are switched "on" and "off". The shorter the voltage and current transition time and voltage and current waveform crossover, the lower the switching energy at switching instants.

15-3-3 Power Loss Estimation Requirements

To accurately predict power loss and temperature rise, accurate simulation of device conduction and switching operation is required. An investigation into how well PSPICE may be used to do this is now conducted. A MOSFET of type IRFP450 will be used throughout the investigation. MOSFET capacitances C_{GD} and C_{DS}, have a big influence on switching behaviour, and it is especially important that they should be properly modelled. The first section is devoted to capacitance simulation in MOSFET's.

15-3-3-1 Non-linear MOSFET capacitance modelling using curve fitting

The PSPICE MOSFET model does not accurately represent C_{GD} and C_{DS} capacitances, which have a strong influence on switching performance.

C_{GD} is highly non-linear and varies with V_{DS}. It has a considerable effect on switching characteristics of the power MOSFET due to Miller Effect. C_{GD} which is equivalent to C_{rss}, (i.e. $C_{GD}=C_{rss}$), increases sharply when the drain-source voltage decreases below 5 V. Therefore, in order to correctly simulate the power MOSFET, it is just as important that C_{GD} should be properly modelled. C_{GD} for the IRFP450 is as given in Fig. 15-9, and is tabulated in App. (15-3) [4].

Malouyans developed a mathematical model for such capacitances for IRF530 and IRF730 [5]. Using the same approach Eq. (15-9) was obtained as a good approximation to Fig. 15-9.

$$C_{GD} = \left(3500 + 413(V_{GE})^{2.95} + 1.2E - 16(V_{GE})^{30.13}\right) / 47.4 \qquad (15\text{-}9)$$

where $V_{GE} = 5 + .9V_{DG} - V_{DG}$. Eq. (15-10) shows another exponential equation that accurately describes C_{GD} as a direct function of V_{DS}:

$$C_{GD} = 1629.96e^{-V_{DS}/3.22274} + 1521.86e^{-V_{DS}/.939372} + 848.04e^{-V_{DS}/18.3257} \qquad (15\text{-}10)$$

Fig. 15-10 shows three graphs; the first comprising discrete C_{GD} as is taken from Fig. 15-9 [see also App. (15-3)]; the second is generated using Eq. (15-9); and the third is generated using Eq. (15-10). It is clear that Eq. (15-10) describes C_{GD} more accurately than Eq. (15-9). Experimentally, C_{GD} for a sample of IRFP450 was measured using a Precision Waynekerr Component Analyser 6425, and is shown in Fig. 15-11. Data for these measurements are given in App. (15-4).

15-3-3-2 Non-linear MOSFET capacitance modelling using look-up tables

Another way of modelling the variable capacitances, C_{GD} and C_{DS}, is as a sub-circuit as shown in Fig. 15-12. The netlist for implementing Fig. 15-12 in PSPICE is given in App. (15-5). The capacitance is replaced by a current source *G1* equals to:

$$i = C_{GD}\frac{dV_{GD}}{dt}$$

where C_{GD} is also a function of V_{GD}. The voltage-controlled voltage-source *E2*, is the C_{GD} value as given in the data sheet. The output of the current-controlled voltage source *H1* is a voltage equal to the current in *C1*. This current equals to *C1* multiplied by the derivative of the output voltage of *E1*, which is the derivative of V_{GD}, i.e. $= 1 \cdot 10^{-9} \cdot \frac{dV_{GD}}{dt}$. The *E2* table takes care of the factor 10^{-9} above, such that, the output of *G1* is exactly the current which will flow in C_{GD} if it is connected between the two nodes 10 and 100. This current of course depends on the voltage between these two nodes.

The same procedure was used to model C_{DS}. *E2* tables for C_{GD} and C_{DS} are shown in App's (15-6) and (15-7), and are plotted in Fig's (15-13) and (15-14). Symbols for

C_{GD} and C_{DS} as shown in Fig. 15-14 were created and used in modelling the IRFP450, as we will see later.

Variations in C_{GS}, on the other hand, have no considerable effect on switching characteristics of the device. Thus, it is considered a constant parameter as a first order approximation, and the value given in PSPICE was not changed.

15-3-4 Effect of Snubber Capacitor

The snubber capacitor and resistor values have a great effect on the shape of the voltage and current waveforms, and thus on the switching power loss. Therefore, to accurately model the circuit, these values should be identical to the ones used in the circuit, including their variations with frequency and voltage, if there is any. During the simulation it was observed that waveforms from the simulation still differ from the practical ones, particularly at transition times.

Further examination to the phenomena, called for the snubber capacitor to be measured at different frequencies and bias voltages. Therefore, the 10 nF ceramic capacitor, used in the circuit, was measured by a precision component analyser. App. (15-8) shows the results, which are plotted in Fig. 15-16, from which we see that the value is 9.4 nF at 20 Hz and zero bias, decreasing to 7.7 nF at 300 kHz and 20 V bias.

To compare this capacitor with different types, a polypropylene capacitor was measured at the same conditions. This type have shown a better stability with frequency and bias voltage with less than 5% change, compared to 18% for the ceramic one.

15-3-5 Thermal Modelling to Predict Junction Temperature

Fig. 15-17 shows the complete "buck" converter, together with power dissipation and thermal models. The model gives junction and case temperatures of the power switch IRFP450, and the power freewheeling diode MUR8100.

Model description

The basic "buck" converter consists of a MOSFET, *M1*, a driver, *V2*, a filter, *L8*, *C1* and *R3* (the *ESR* of *C1*), and a load *R6* draws a load current of 4 A. The input voltage, *V1* = 200 V. *R1* models the R_{DSon} of *M1*, *C2* and *C3* are voltage-dependant capacitors as described in Sec. (15-3-3) above. *L1*, *L2* and *L3* are parasitic inductances inside *M1*. These parasitic elements have shown a great effect on switching waveforms, and they should be accurately modelled. *R5*, *C5* and *R6*, *C6* are snubbers across *M1* and *D1*, with *L5* and *L6* being the stray inductances of their leads. *F1* and *F2* are used to measure the current through *M1* and *D1*, while *E5* and *E4* give outputs equal to the product of the voltage across *M1* and *D1* with the current through them, i.e. the power dissipation. Since the power dissipation is $V \cdot I$, any negative sign of one value will give negative power. In fact, this power is not given to the device but dissipated in it, irrespective of whether it is positive or negative. Therefore, absolute value of the power should be taken to represent the real power dissipation in the device. *G1* and *G2* take care of this function. *C9-C14* and *R10-R15* represent the thermal impedance model of the transistor, while *C16-C22* and *R16-R22* represent the thermal impedance model of *D1*. These values were obtained as described in Sec. (15-2). *V4* and *V5* represent the ambient temperature, while *V6* and *V7* represent the temperature across the heat sink and the insulated washer, taking into account the added thermal grease and a smooth and clean interface.

To calculate the average power dissipation, Eq. (15-11) is used:

$$Pav = \frac{1}{t}\int Pidt \qquad (15\text{-}11)$$

where *t* is the simulation time, and *Pi* is the instantaneous power dissipation. Eq. (15-11) can be solved using *F3*, *C15*, *R23*, *E2* and *R26* for average power dissipation in *M1*, and *F4*, *C23*, *R24*, *E3* and *R27* for average power dissipation in *D1*. To find the steady state temperature, the average power value should be multiplied by the thermal resistance, which is 3.1° C/W for IRFP450 and 2.5° C/W for MUR8100. This value can be seen across *R26* for *M1*, and across *R27* for *D1*. At input voltage and

load current values of VI = 200 V and I_L = 4A, 7.4 W was dissipated in the switch, and 3 W was dissipated in the diode.

15-3-6 Core Loss Modelling

Core losses consists mainly of hysteresis losses and Eddy-current losses.

15-3-6-1 Hysteresis loss

Hysteresis losses are proportional to the area of the $B-H$ loop or the hysteresis loop, and may be given by: P_h = area of $B-H$ loop$\cdot A_e \cdot l_e$. This can be rewritten as:

$$P_h = V_e \cdot \oint H dB \tag{15-12}$$

To solve Eq. (15-12), calculation of B and H is required. This was implemented in PSPICE using ten circuit components as shown in Fig. 15-18. The components used to calculate hysteresis power loss are *V3, H3, G1, C2, R19, G6, L2, G2, C3* and *R20.*

If Eq. (15-12) is converted to time domain, instead of B domain, the model can be simplified. To do so, we have the following basic equations:

$$H = \frac{i_M \cdot N}{l_e} \tag{15-13}$$

$$v = N\frac{d\phi}{dt} = N \cdot A_e \cdot \frac{dB}{dt} \Rightarrow \frac{dB}{dt} = \frac{v}{N \cdot A_e} \tag{15-14}$$

Eq. (15-12) can be rewritten, for continuous flux, as:

$$P_h = V_e \cdot \oint H \frac{dB}{dt} \cdot dt \tag{15-15}$$

Substituting Eq's (15-13) and (15-14) in (15-15) results in:

$$P_h = V_e \cdot \int \frac{i_M \cdot N}{l_e} \cdot \frac{v}{N \cdot A_e} dt = \int i_M \cdot v dt \qquad (15\text{-}16)$$

which is logically true. The reason for this is that when simulating the transformer by its equivalent circuit, hysteresis is represented by the magnetising inductance, L_M, which conducts the current i_M that is responsible of maintaining the flux in the core. Therefore, the power loss in this inductance is just what we have obtained in Eq. (15-16). Eq. (15-16) means that there is no need to calculate B and H in order to find the hysteresis loss. Fig. 15-18 shows how this equation can be implemented in PSPICE, where we see that only five components are needed now, compared to ten in the previous model. These components are *V3, V4, G7, C4* and *R33*. Simulation has shown that both models give exactly the same results.

15-3-6-2 Eddy-current loss

Eddy-current loss is generally given by:

$$P_e = \frac{d^2}{3\rho}(\frac{dB}{dt})^2 V_e = \frac{d^2}{3\rho} V_e (\frac{v}{NA_e})^2 = \frac{d^2 l_e}{3\rho N^2 A_e} v^2 \qquad [\text{W/m}^3] \qquad (15\text{-}17)$$

If we have a core size EC41/19/12, type FX3730 made of 3C8 material grade, the following parameters may be specified:

l_e =.0893 m, $A_e = 121e^{-6}$ m^2, $\rho = 1$, and $d \approx 5.85e^{-3}$ m.

If $N = 51$, as used in simulation, then we have the following expression for Eddy-current loss:

$$P_e = 3.2368 \cdot v^2 \qquad (15\text{-}18)$$

where v is the voltage applied across the primary.

15-3-6-3 The average value of core losses

The value obtained from Eq. (15-16) is the hysteresis energy absorbed by the core, which increases time. This energy is measured in Joule. To find the power, this

value should be divided by simulation time, which is available as a variable in PSPICE. The same applies on Eddy-current loss where the value given in Eq. (15-18) is the instantaneous power. In order to get the average power, this value should first be integrated over time, and then divided by time. Fig. 15-19 shows the complete circuit used to model hysteresis and Eddy-current losses. Fig. 15-20 shows hysteresis energy during two cycles, while Fig. 15-21 shows hysteresis and Eddy-current power loss for the circuit of Fig. 15-19.

CHAPTER THIRTEEN REFERENCES

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5. S. Malouyans, "SPICE computer models for HEXFET power MOSFET's", Application Note 975B, IR.
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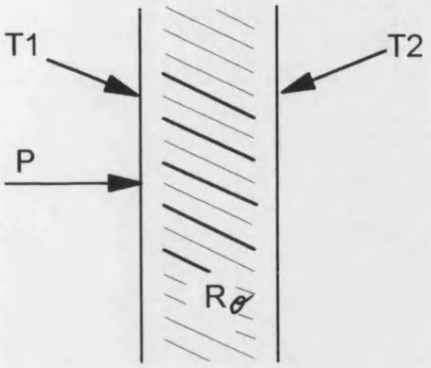


Fig. 15-1

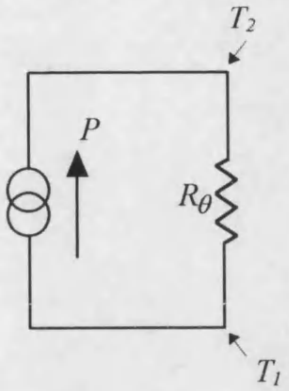


Fig. 15-2

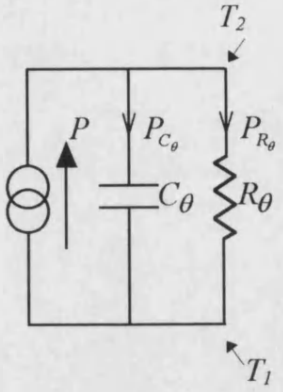


Fig. 15-3

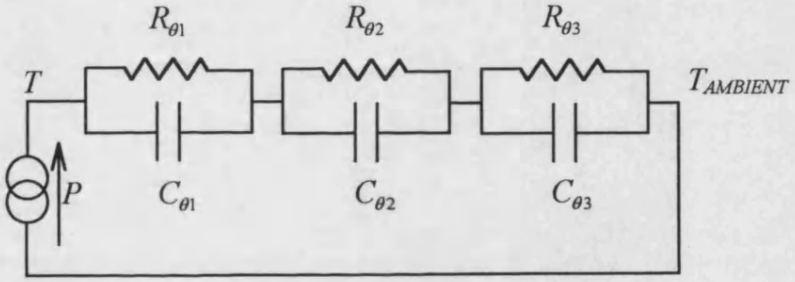


Fig. 15-4 Three network branches to simulate a thermal impedance curve

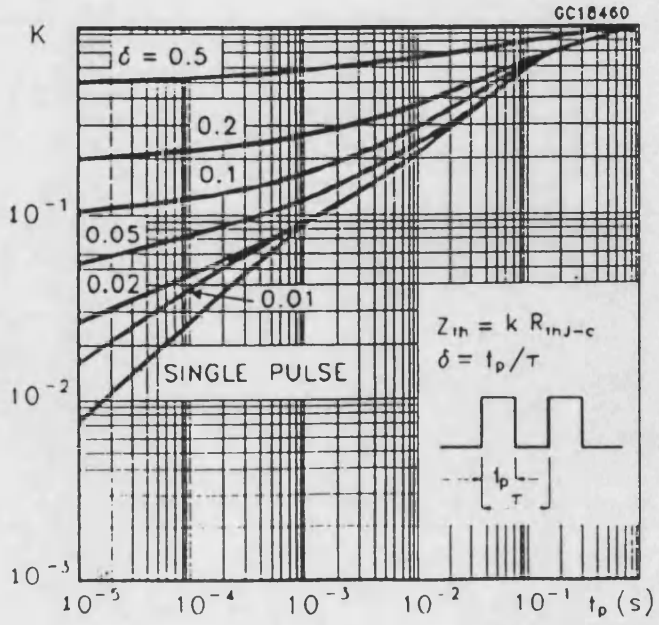


Fig. 15-5 The normalised thermal impedance curve for IRFP450 [4]

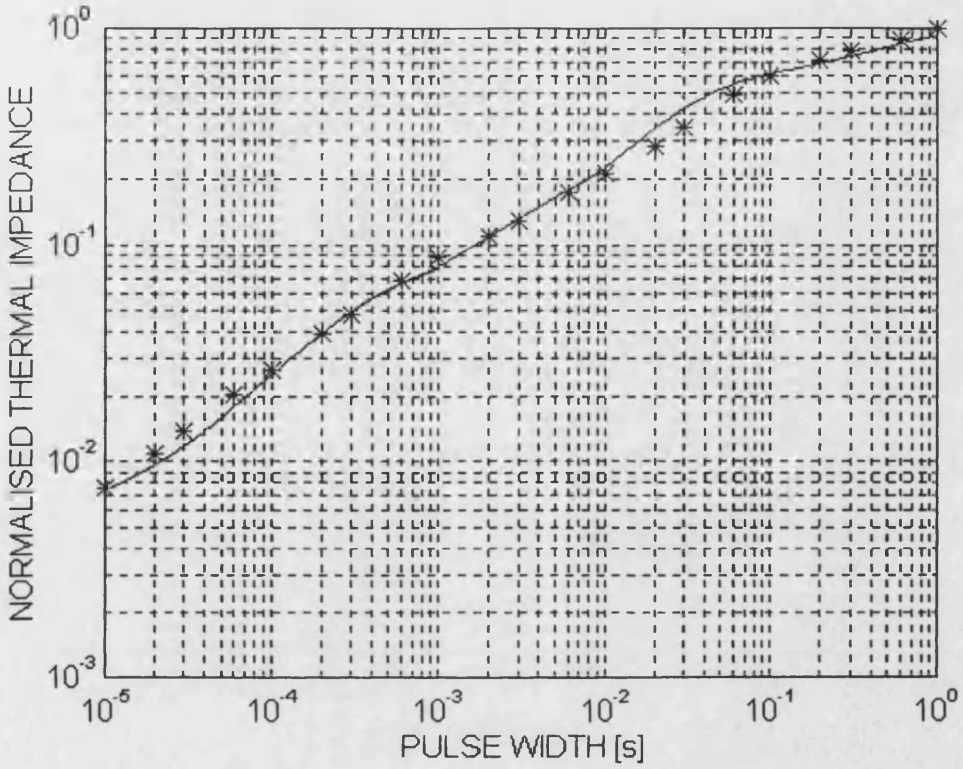


Fig. 15-6 The normalised thermal impedance curve using Eq. (15-7) for four network branches

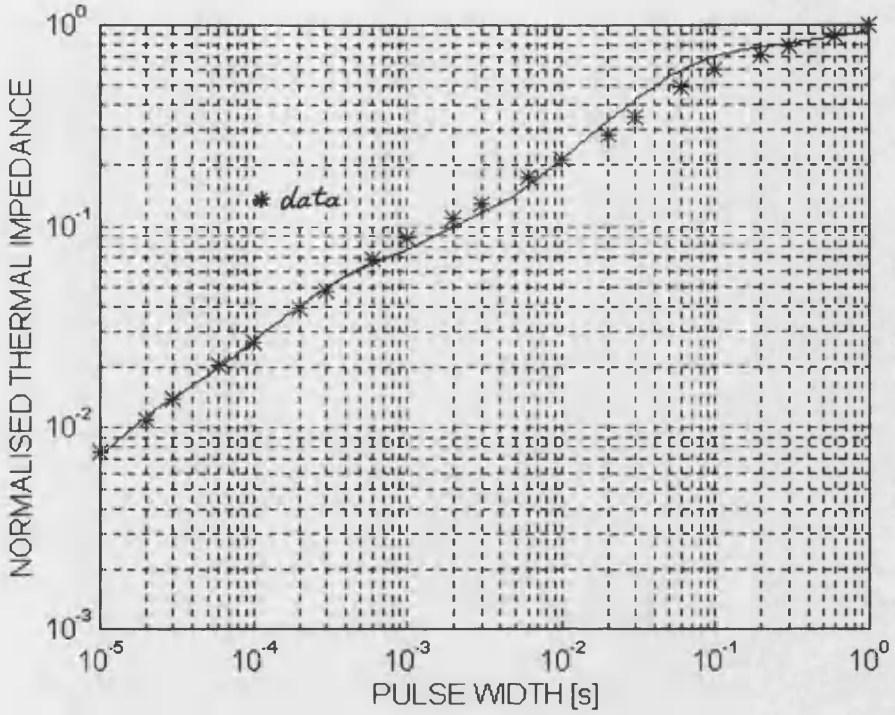


Fig. 15-7 The normalised thermal impedance curve using Eq. (15-7) for five network branches

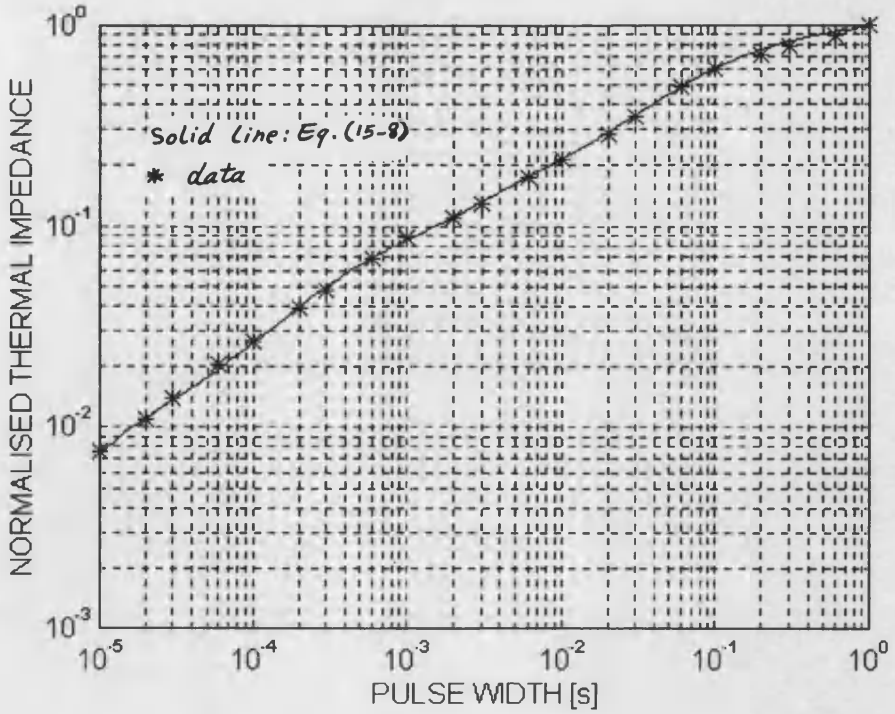


Fig. 15-8 Normalised thermal impedance: data and Eq. (15-8)

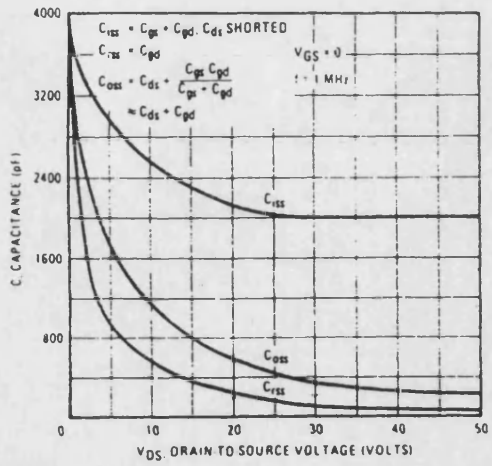


Fig. 15-9 C_{rss} variations with V_{DS} as given in data sheet [4]

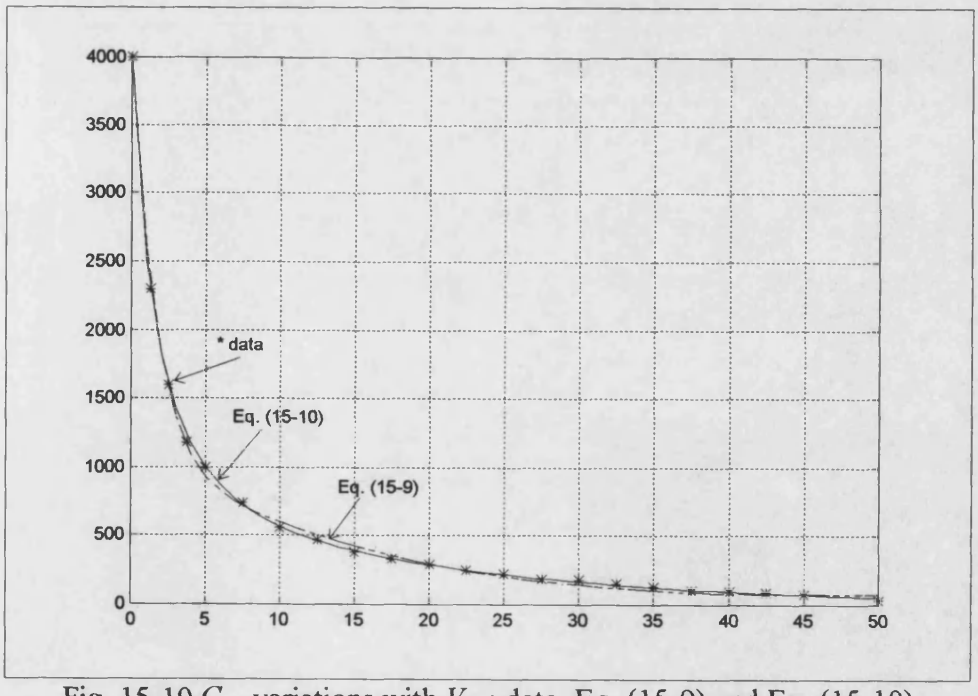


Fig. 15-10 C_{rss} variations with V_{DS}: data, Eq. (15-9) and Eq. (15-10)

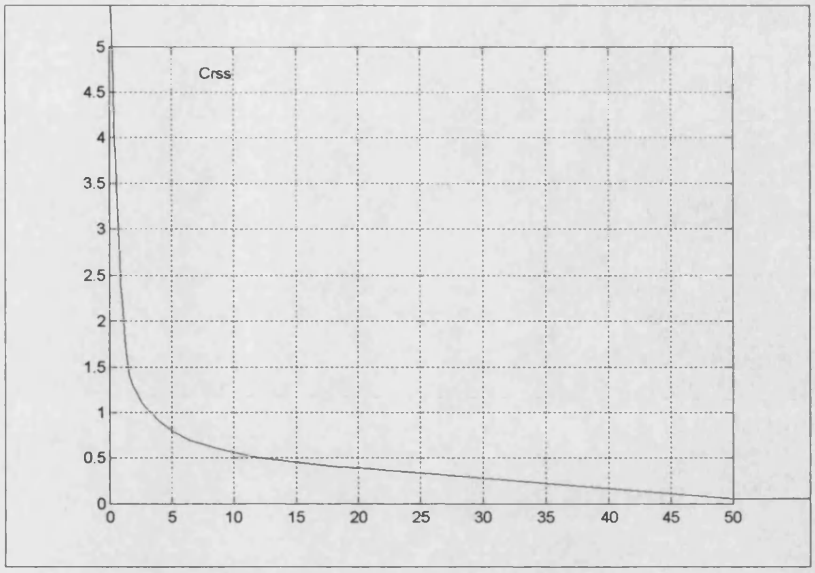


Fig. 15-11 C_{rss} variations with V_{DS} as measured by a precision component analyser [see App. (15-4)]

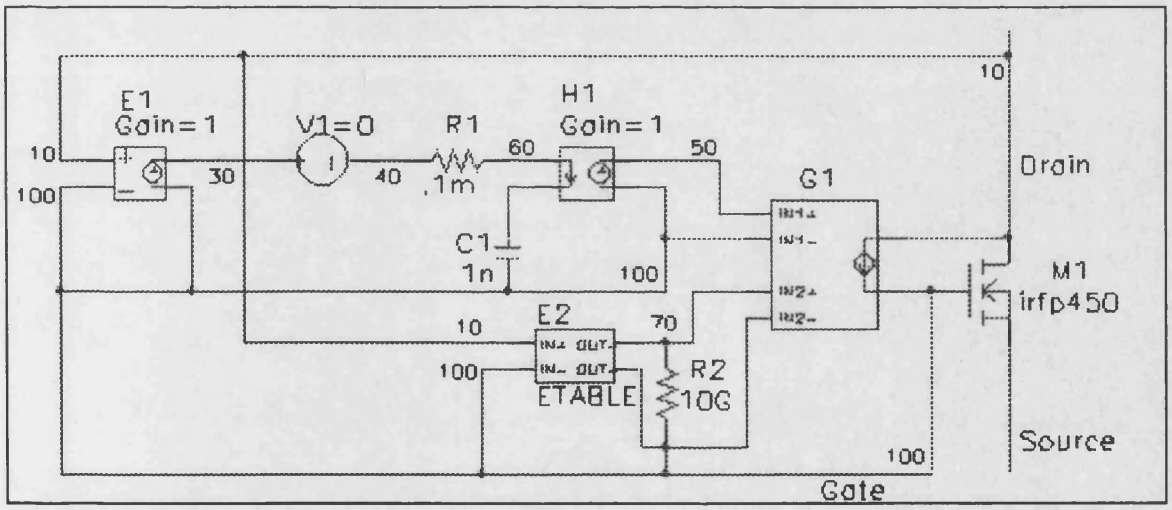


Fig. 15-12 Sub-circuit to model C_{GD} or C_{DS} of a MOSFET

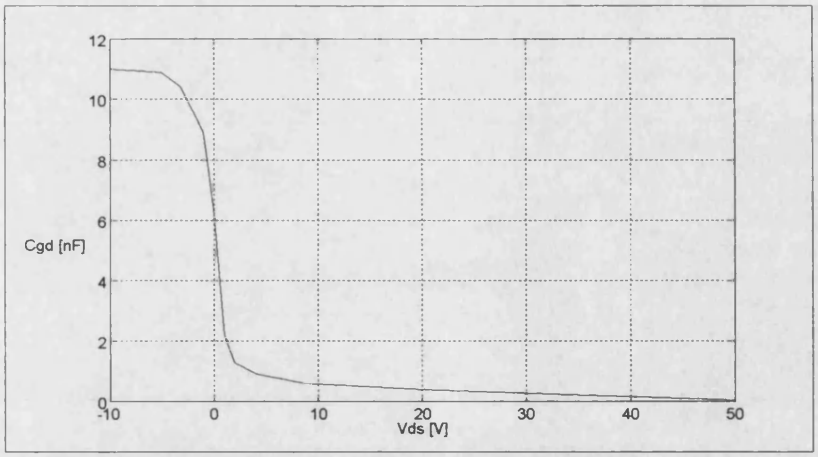


Fig. 15-13 C_{GD} variations with V_{DS} which is used in Simulation [see App. (15-6)]

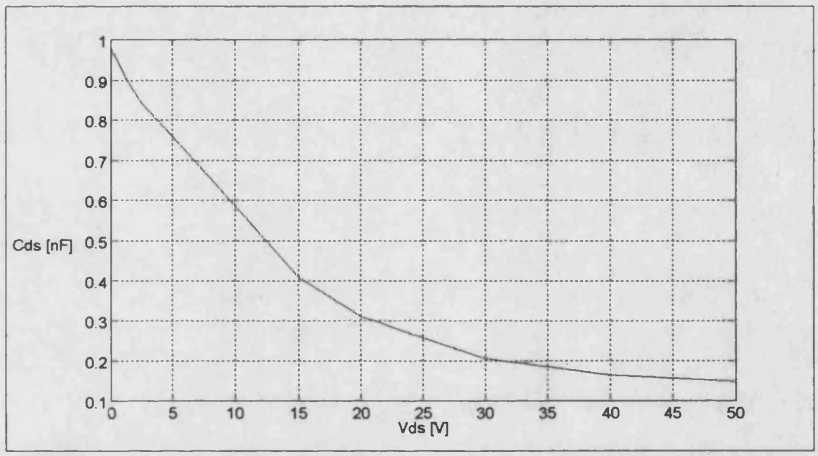


Fig. 15-14 C_{DS} variations with V_{DS} which is used in Simulation [see App. (15-7)]

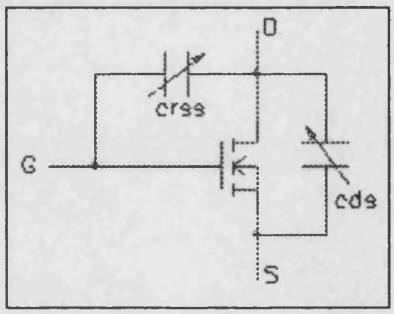


Fig. 15-15 Symbols for C_{rss} and C_{DS}

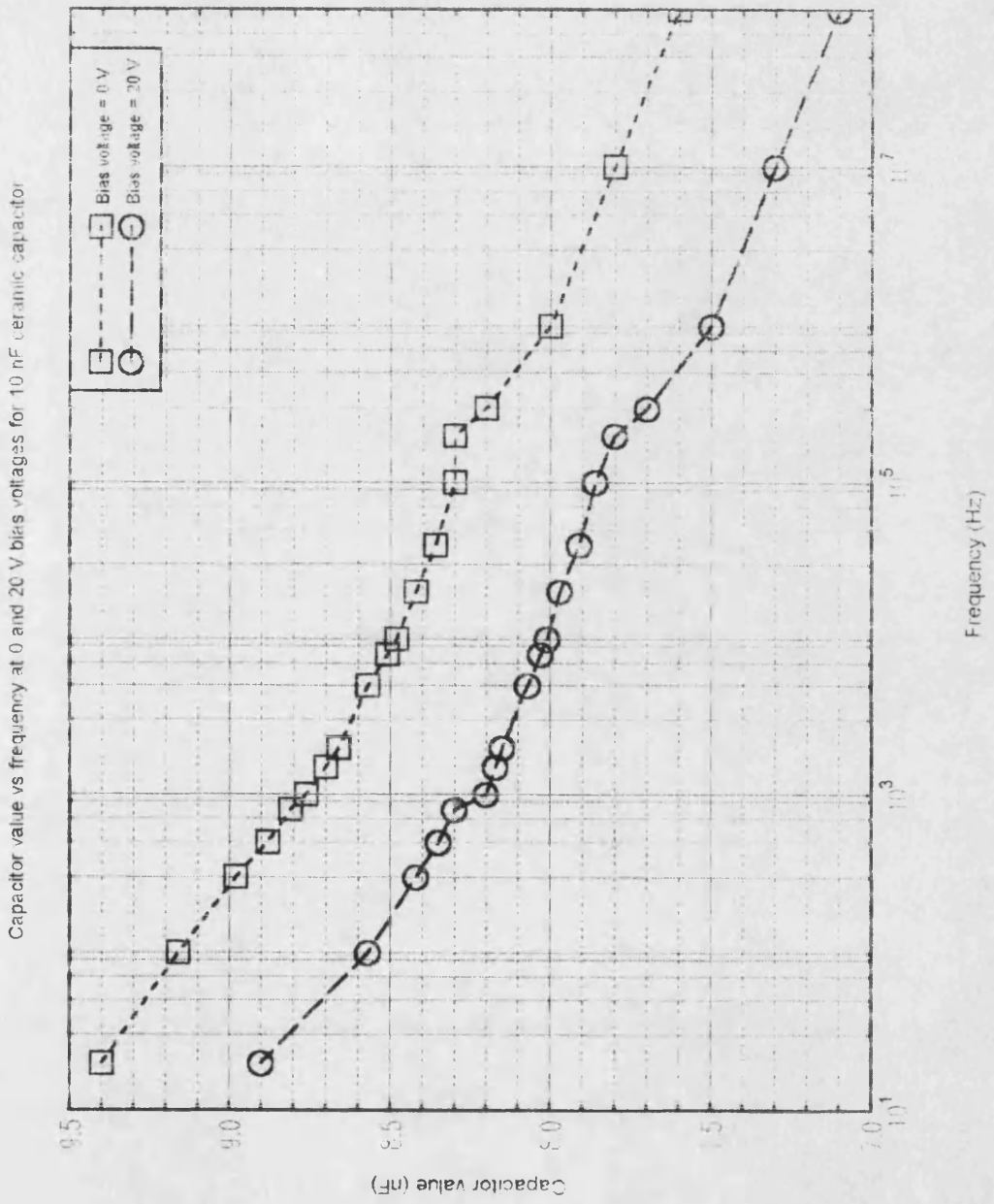


Fig. 15-16 Capacitance values versus frequency at bias=0 and 20 V for 10 nF ceramic capacitor

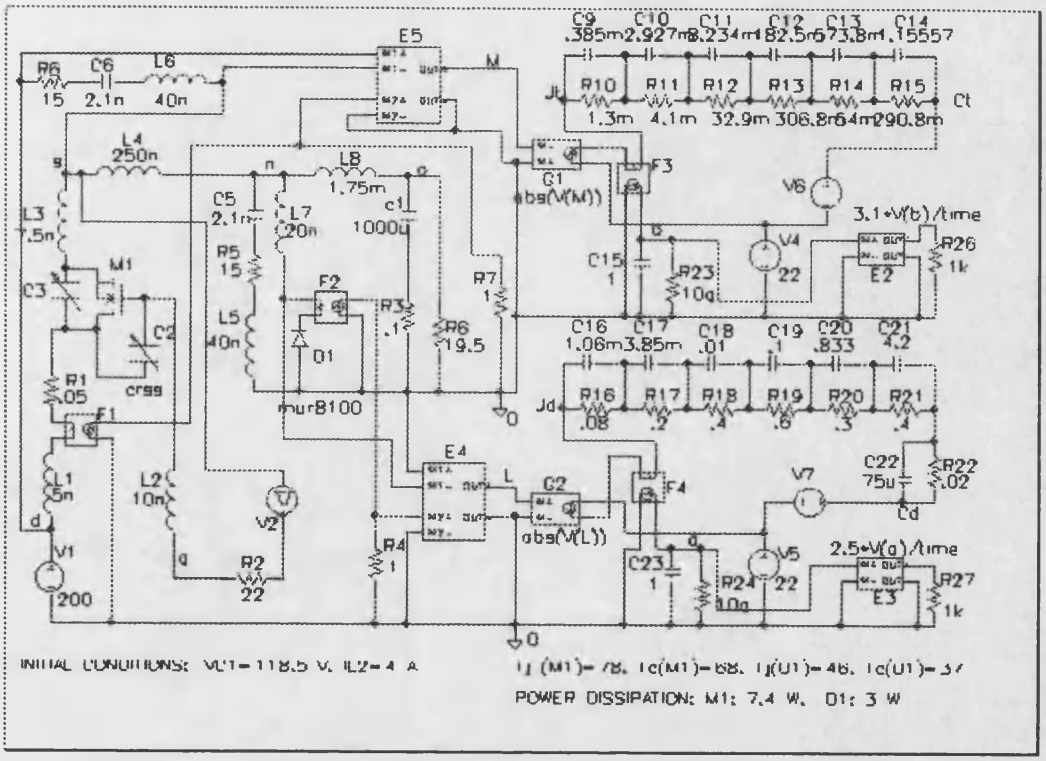


Fig. 15-17 Power dissipation model for IRFP450 and MUR8100

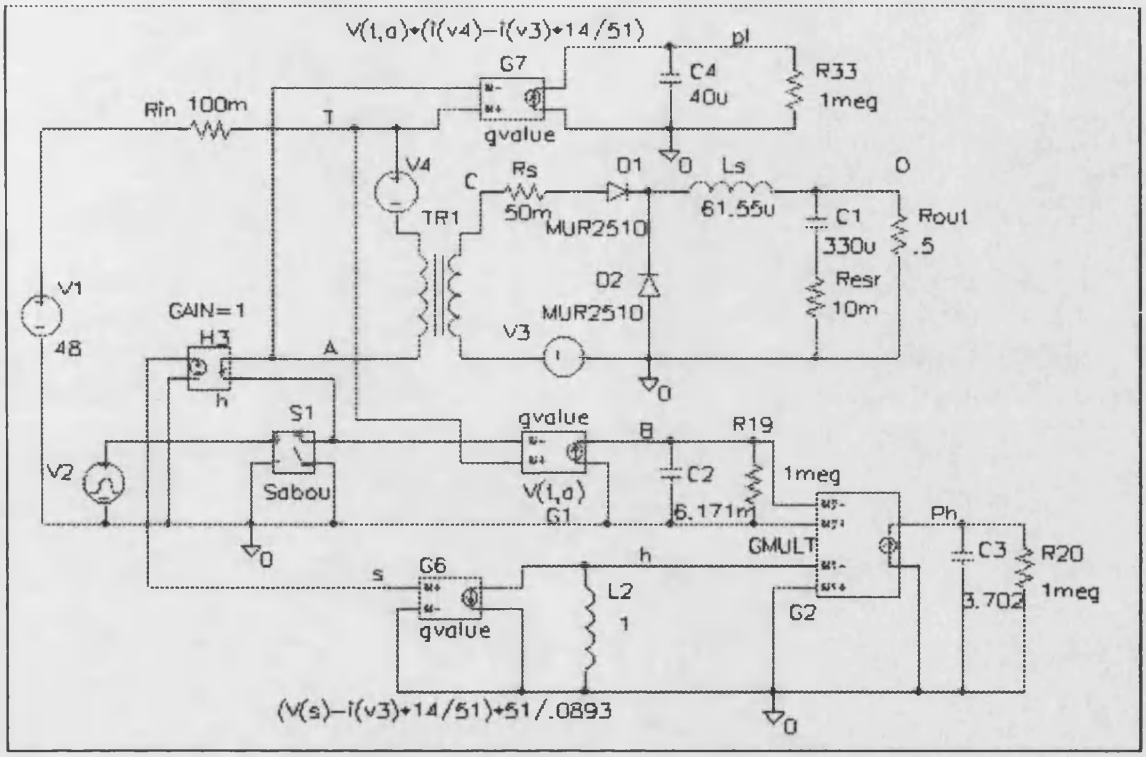


Fig. 15-18 Calculating hysteresis losses from B and H values

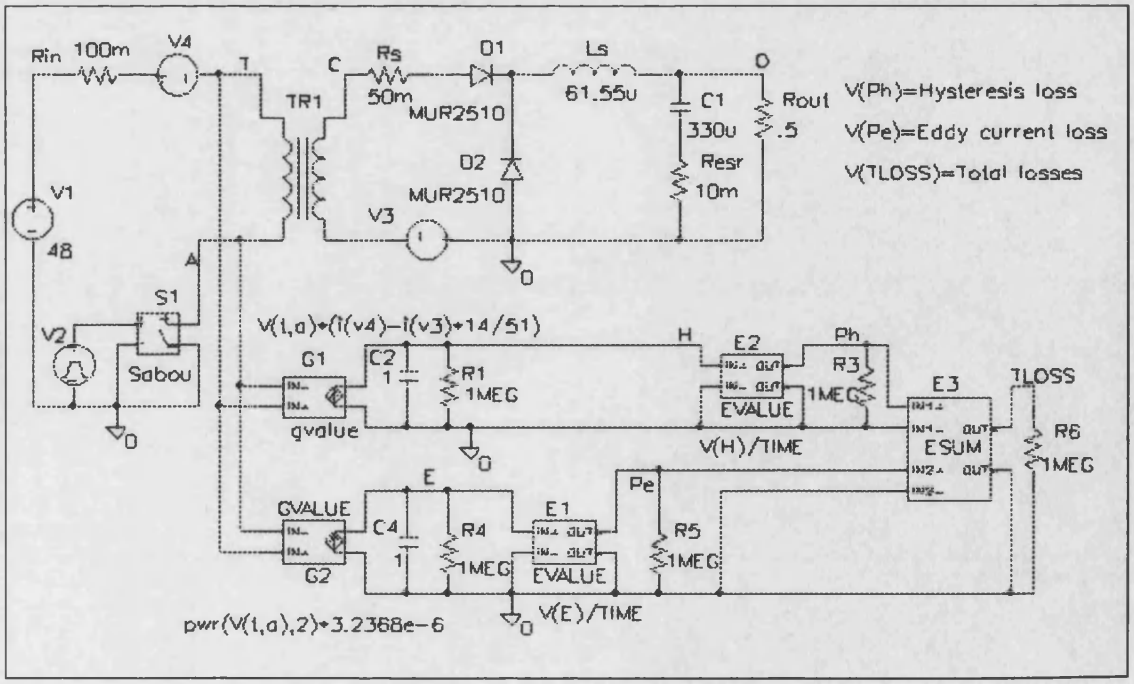
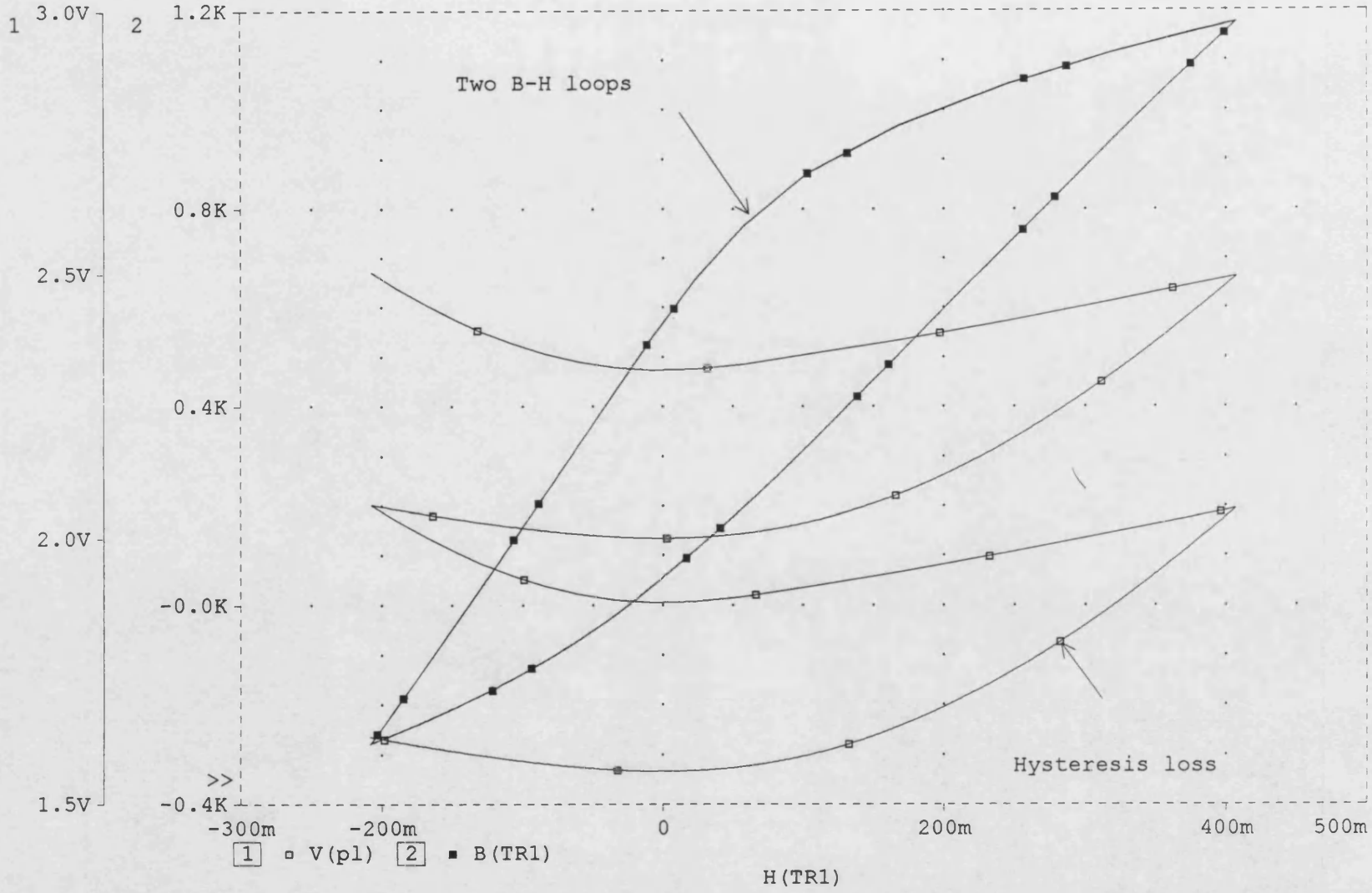


Fig. 15-19 Hysteresis and Eddy-current losses modelling



Date: May 14, 1996

Fig. 15-20 Hysteresis energy during two cycles

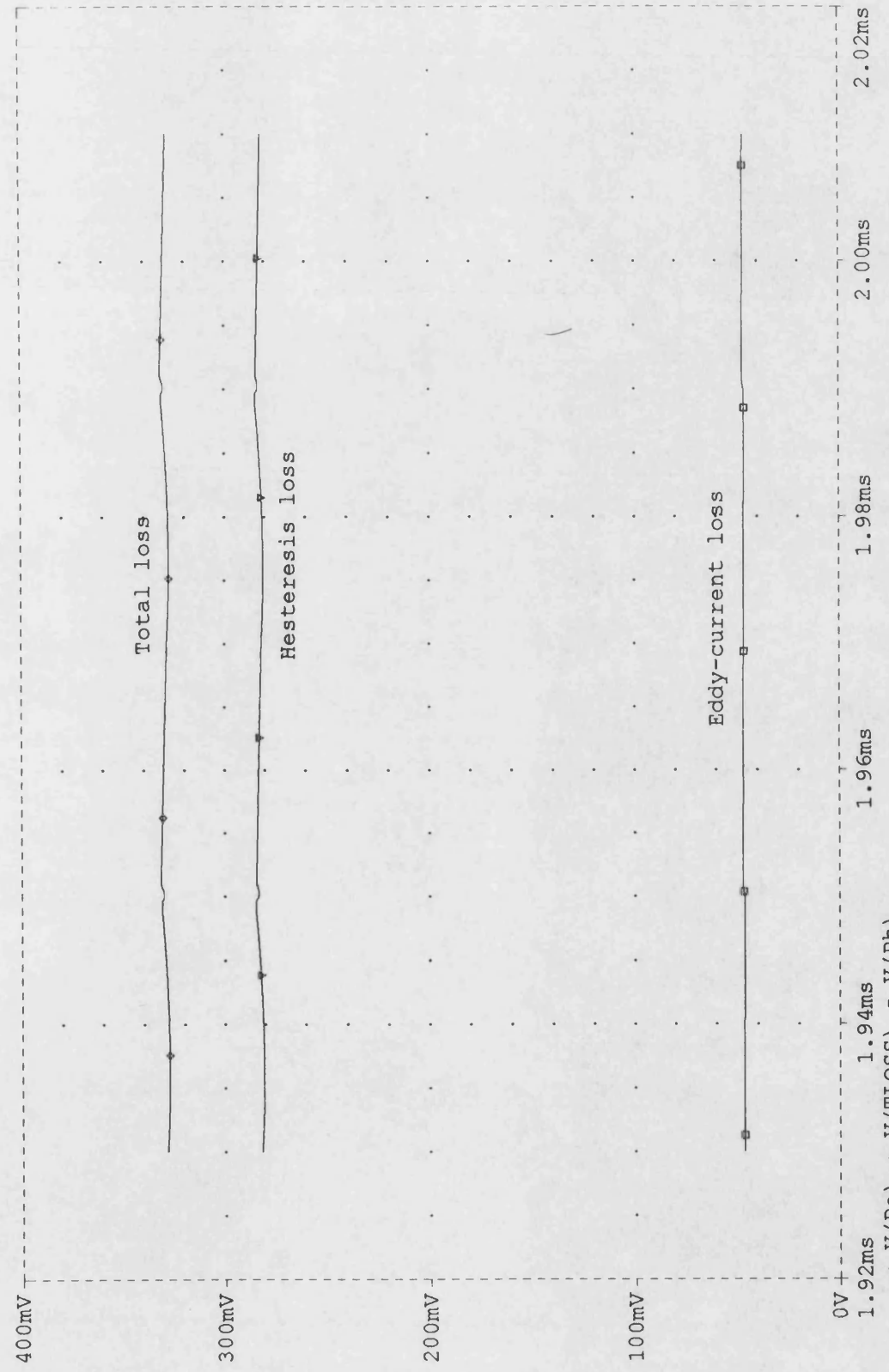


Fig. 15-21 Hysteresis and Eddy-Current power loss

CONCLUSION AND FURTHER WORK

16-1 CONCLUSION

This work generally divides into two main parts; the first is the weakness of dc/dc and dc/ac converters and how they can be solved or their effects be reduced; the second is modeling and simulation of several switch-mode power converters, including transformer and thermal modeling.

The first part reviewed the principles of operation of the main and commonly-used transformer-isolated dc/dc and dc/ac converter topologies, and covered push-pull, flyback, half-bridge, full-bridge and forward converters including single-ended, double-ended and interleaved forward converters. Attempts have been made to improve the performance of these topologies. Therefore, the main drawbacks have been highlighted and solutions to some of these drawbacks have been suggested. The solutions are supported by graphs and tables and simulated by PSPICE before the practical circuit has been built. Afterwards, the practical circuit is designed and practically tested, and results from the circuit are analyzed and compared to the theory. A new topology has been introduced and its merits and limitations have been discussed.

The main points presented in the first part are:

1. Studying the effect of the reset winding turns in single-ended forward converters on the peak primary current and the maximum reverse voltage which the power semiconductor switch must withstand. Three graphs have been plotted and showed that the optimum reset winding turns for minimum switched VA is equal to the number of primary winding turns (Fig's 3-3 to 3-5).
2. The effect of the primary and secondary stray and leakage inductance in single-ended forward converter has been illustrated and equations for the voltage spikes induced due to this inductance have been derived. The study has shown that the primary stray inductance has a double effect on the voltage spike magnitude compared to primary leakage inductance, while the reset and secondary windings leakage inductance has no effect on the induced voltage spike.
3. A method employing the IR2110 MOSFET driver to eliminate the driving transformer from double-ended forward converters has been introduced and compared to what has been reported elsewhere. The circuit used to realize this has been thoroughly discussed and simulated in PSPICE and then practically tested. The effect of the dc input voltage and the load current on the limitations of this method is investigated.
4. Flux imbalance in push-pull dc/dc and dc/ac converters has been thoroughly examined. Flux imbalance description, reasons for flux imbalance and methods to reduce its effect have also been presented. A new method employing magnetising current-mode control has been introduced first through simulation and then practically tested and compared with the conventional primary current-mode control. The results show that no flux imbalance can occur at all load conditions when the magnetising current is used to control the power switches, while it may occur when primary current-mode control is used at no- or light- loads. Flux imbalance in other dc/dc converters has also been presented.
5. A new topology employing a three-phase transformer in dc/dc converters has been introduced and applied to a push-pull dc/dc converter. The control

circuit for this converter has been designed and the converter has been practically tested. It has been shown theoretically and through PSPICE simulation that the voltage stress on the "off" power switches is 1.5 times the input dc voltage compared to twice the voltage in conventional dc/dc push-pull converters. Practically, it has been found that this value depends on the circuit layout and the resistor and capacitor snubber values connected across the rectifying diodes. The poor utilization of the power switches and transformer windings makes this technique not suitable except at high dc voltages when the conventional circuits are not used.

6. Low-frequency dc/ac inverters have been examined in detail; that is power device current and voltage ratings have been derived and the conduction and switching power losses for all topologies have been estimated. It has been found that low-frequency full-bridge dc/ac inverters offer the maximum efficiency.
7. A full-bridge dc/ac inverter has been studied and designed, and the destruction of the power semiconductor switches have been systematically investigated. A new idea to prevent multiple switching of the power switches due to noise has been introduced. The effect of transformer interwinding capacitance is also investigated, and a method to reduce this effect is first simulated and then applied into the inverter. It has been shown that placing the output filter at the primary side considerably reduces the noise at the output caused by the interwinding capacitance. The effect of the snubber resistor values on the energy loss in the snubber resistors have been thoroughly investigated through deriving the required equations and confirmed by PSPICE simulation. It has been shown that when the snubber resistor equals or larger than twice the equivalent primary load resistance, all the energy stored in the snubber capacitor is dissipated in the snubber resistor.
8. The effect of parasitic elements, such as stray and leakage inductance, magnetising inductance and equivalent series resistance, *ESR*, of capacitors, on the function of switch-mode power converters is discussed. Ways of reducing these elements are presented and a new circuit to measure the *ESR* is designed and is being used for *ESR* measurements.

In addition to examining dc/dc and dc/ac converters practically, comprehensive simulation is used throughout this work. Therefore, the main points which are covered in the second part are as follows:

1. PSPICE problems have been highlighted and MATLAB circuit simulator is suggested as an alternative to PSPICE in some situations where PSPICE fails. The advantages of MATLAB compared to PSPICE in such cases is also presented.
2. Attempts have been made to exploit the MATLAB numerical simulator to demonstrate the ability of such simulators to model and simulate electrical circuits including transformers. A starting point was the MATLAB hysteresis modeling first through using look-up tables and then curve-fitting techniques. The limitations of the model is also discussed.
3. Comprehensive work has been spent on PSPICE single- and three-phase transformer modeling to help simulating transformer-isolated switch-mode power supplies. The effect of remanent flux in transformers and how the steady-state flux can be quickly established when simulating single- and three-phase transformers in PSPICE have been illustrated.
4. Several transformer-isolated dc/dc converter topologies including a pure resistive-load circuit, single-ended forward converter and flyback converter, were simulated in MATLAB using the developed single-phase transformer model.
5. The principle of operation of the three-phase transformers has been discussed, equations to calculate material saving when these transformers are used were derived and examples for different core geometries were given.
6. An important issue in switching power supplies which is the thermal modeling has been discussed. In order to model the junction and case temperature of power semiconductors, accurate voltage and current waveforms have been obtained by simulation. Therefore, MOSFET non-linear capacitances are properly modeled, together with thermal impedance curves of these semiconductors as given in the data sheets. Core loss modeling, including hysteresis and Eddy-current losses are also modeled.

Finally, other useful topics have been added in the appendices which cover the calculation of effective and actual volume of cores, calculation of the time constant for estimating the time required by an inductor or a transformer to reach the steady-state flux conditions, deriving the equations relating the secondary voltage to the load current for different load configurations and how it can be implemented in MATLAB, a general procedure for finding an equivalent circuit model for any thermal impedance graph and, finally, MATLAB programs for some of the graphs shown in this report.

16-2 FURTHER WORK

Several high-frequency dc/ac inverters should be designed at specific power and switching frequency, and power losses may then be practically measured and compared to each other to verify the calculated values and conclusions presented in this report.

Further work is required to establish an easy method of estimating transformer-volume as a function of power and switching frequency, and transformer weight and volume saving when using high-frequency techniques, to assist designers establish the optimum inverter operating frequency.

Other drawbacks in other dc/dc converters have to be examined and solutions have to be found in order to improve their performance and extend their application area.

As mentioned in MATLAB hysteresis modeling, there is oscillation in the closed loop of the transformer model due to a step in B values at the far ends of the hysteresis loop which causes μ to have very high values.

Another limitation of the model stems from the fact that the procedure used to extract the minor loops from the major loop does not inherently seem to work well at very small minor loops, and/or for converters that use only one half of the hysteresis loop such as forward and flyback converters.

Therefore, some work is still required in MATLAB hysteresis and transformer models to enable it to work at any core flux condition.

Three-phase transformers also need be modeled in MATLAB and the PSPICE three-phase transformer model should also be improved if it is required to simulate three-phase circuits.

A library containing MATLAB component models has to be increased to facilitate simulating electrical circuits in MATLAB.

APPENDIX 3-1 DATA SHEET FOR THE MOSFET DRIVER

Data Sheet No. PD-6.011

INTERNATIONAL RECTIFIER IOR

HIGH VOLTAGE MOS GATE DRIVER

IR2110

General Description

The IR2110 is a high voltage, high speed MOS-gated power device driver with independent high side and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS outputs or with LSTTL outputs using pull-up resistors. Output drivers use low impedance totem-pole arrangement designed for low cross-conduction current spike. Propagation delays for the two channels are matched to simplify use in high frequency application. The floating channel can be used to drive a N-channel power MOSFET or IGBT in the high side configuration that operates off high voltage rail up to 500 volts.

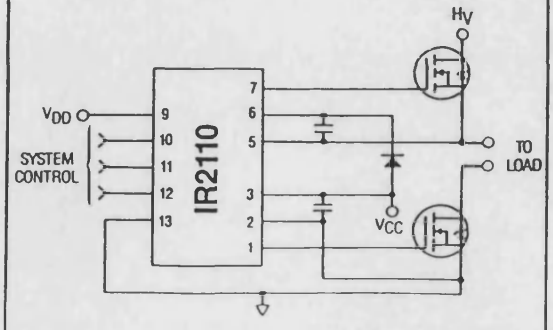
Applications

- High frequency switch-mode power supply
- DC and AC motor drives
- Electronic lamp ballast
- Battery charger
- Induction heating and welding
- Switching amplifier

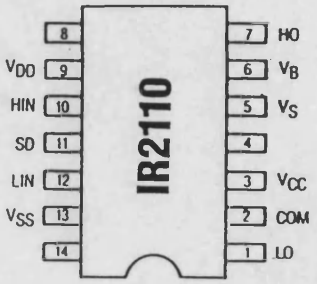
Features

- Floating supply designed for bootstrap operation
  - — Operating offset range from −4 to +500V
  - — dv/dt immunity rated at ±50V/ns
  - — Quiescent power dissipation of 1.6mW at 15V
- Wide output operating gate drive supply range from 10 to 20V
- Separate logic supply to interface with logic signal
  - — Operating supply range from 5 to 20V
  - — Logic and power ground operating offset range from −5 to +5V
- CMOS Schmitt-triggered inputs with hysteresis and pull-down
- Cycle by cycle edge-triggered shutdown logic
- Undervoltage lockout with hysteresis for both channels
- Output totem-pole driver designed to drive MOS-gated power devices
  - — Peak current capability at 2A minimum
  - — Switching time of 25ns typical into 1000pf load
- Matched propagation delay time for both channels
  - — Typical 120ns turn-on delay and 94ns turn-off delay
  - — Maximum rated matching differential of ±10ns
- Latch immune CMOS. Withstand >2A reverse current at I/O pins

Typical Connection



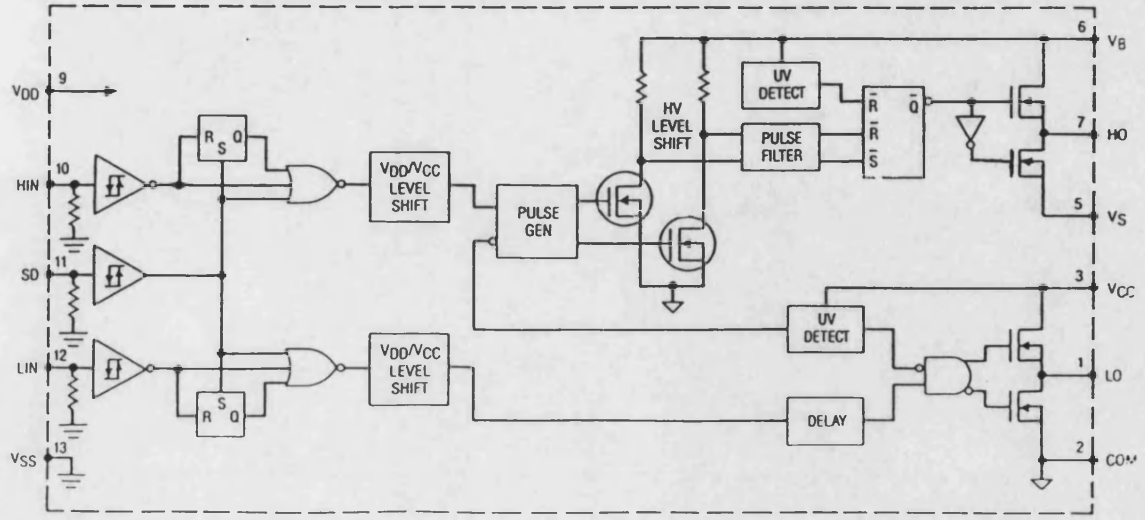
Pinout Assignment



For mechanical specifications see back page

		T_J = 25°C			T_J = −55 to 150°C				
Symbol	Parameter	Min	Typ	Max	Min	Max	Units	Test Conditions	Fig.
V_{IH}	Logic "1" Input Volta	3.1	—	—	3.3	—	V	V_{DD} = 5V	Fig. 4
		6.4	—	—	6.8	—		V_{DD} = 10V	
		9.5	—	—	10	—		V_{DD} = 15V	
		12.6	—	—	13.3	—		V_{DD} = 20V	
V_{IL}	Logic "0" Input Voltage	—	—	1.8	—	1.7		V_{DD} = 5V	
		—	—	3.8	—	3.6		V_{DD} = 10V	
		—	—	6	—	5.7		V_{DD} = 15V	
		—	—	8.3	—	7.9		V_{DD} = 20V	
V_{OH}	High Level Output Voltage, V_{BIAS}-VO	—	0.7	1.2	—	1.5	V	V_{IN} = V_{IH}, I_O = 0A	Fig. 10
V_{OL}	Low Level Output Voltage, VO	—	—	0.1	—	0.1		V_{IN} = V_{IL}, I_O = 0A	
I_{LK}	Offset Supply Leakage Current	—	—	50	—	250	μA	V_B = V_S = 500V	Fig. 5
I_{QBS}	Quiescent V_{BS} Supply Current	—	125	230	—	500		V_{IN} = V_{IH} or V_{IL}	Fig. 6
I_{QCC}	Quiescent V_{CC} Supply Current	—	180	340	—	600		V_{IN} = V_{IH} or V_{IL}	Fig. 7
I_{QDD}	Quiescent V_{DD} Supply Current	—	5	30	—	60		V_{IN} = V_{IH} or V_{IL}	
I_{IN+}	Logic "1" Input Bias Current	—	15	30	—	70		V_{IN} = 15V	Fig. 8
I_{IN-}	Logic "0" Input Bias Current	—	—	1	—	10		V_{IN} = 0V	
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	7.7	8.7	9.7	—	—	V		Fig. 9
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	7.3	8.3	9.3	—	—			
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	7.6	8.6	9.6	—	—			
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	7.2	8.2	9.2	—	—			
I_{O+}	Output High Short Circuit Pulsed Current	2	—	—	—	—	A	V_{OUT} = 0V, V_{IN} = 15V, PW <= 10 μs	
I_{O-}	Output Low Short Circuit Pulsed Current	2	—	—	—	—		V_{OUT} = 15V, V_{IN} = 0V, PW <= 10 μs	

Functional Block Diagram



APPENDIX 3-2 CALCULATING THE BOOTSTRAP CAPACITOR VALUE

If a voltage source, V_{CC}, is connected across the bootstrap capacitor C_{ext}, the charge stored in the capacitor is:

$$Q = C_{ext} V_{CC} \tag{A3-1}$$

If the capacitor is now connected across the input capacitance of the MOSFET, C_{ioss}, the equivalent capacitance value will be:

$$C_{eq} = C_{ext} + C_{ioss} \tag{A3-2}$$

The resultant voltage in this case will be:

$$V = \frac{Q}{C_{eq}} = \frac{Q}{C_{ext} + C_{ioss}} \tag{A3-3}$$

To ensure that the resultant voltage is sufficiently large to keep the MOSFET "on", this voltage should be at least twice the threshold level, V_{TH}, of the MOSFET, i.e.

$$V \geq 2V_{TH} \tag{A3-4}$$

Substituting Eq. (A3-4) in Eq. (A3-3) gives:

$$Q \geq 2V_{TH}(C_{ext} + C_{ioss}) \tag{A3-5}$$

Using Eq. (A3-1), a formula for C_{ext} can be obtained:

$$C_{ext} V_{CC} \geq 2V_{TH} C_{ext} + 2V_{TH} C_{ioss}$$

$$C_{ext}(V_{CC} - 2V_{TH}) \geq 2V_{TH}C_{ioss}$$

$$C_{ext} \geq \frac{2V_{TH}C_{ioss}}{V_{CC} - 2V_{TH}} \qquad \text{(A3-6)}$$

For example, if V_{TH} = 4 V, C_{ioss} = 12 nF, V_{CC} = 12 V, then:

$$C_{ext} \geq \frac{2 \cdot 4 \cdot 12}{12 - 8} = 24 \text{ nF}$$

Practically, C_{ext} must be well above the calculated value to accommodate for any leakage current and any added capacitance from D_1 and the previous circuit. An acceptable value would be 100 nF for most applications.

Eq. (A3-6) states that using a MOSFET of higher input capacitance and threshold voltage, and/or using a lower supply voltage, V_{CC}, requires higher bootstrap capacitor. Also, Eq. (A3-6) shows that C_{ext} does not depend on the frequency and duty-cycle, as published in [4].

In fact, the frequency and the duty-cycle indirectly affect the operation of the converter that uses this method of driving MOSFET's. The bootstrap capacitor charges during the "on" time of the lower MOSFET in half- and full-bridge circuits, and during the "off" time in double-ended forward circuits. The voltage across the bootstrap capacitor depends, in addition to its capacitance value and the supply voltage V_{CC}, on the time through which the capacitor charges. If this time is short, i.e. if the duty-cycle is small and/or the frequency is high, there is a tendency that the capacitor does not charge to the required value, as is shown practically.

When selecting C_{ext}, a compromise has to be struck between two conflicting requirements:

if C_{ext} is too small, it will discharge below $2V_{TH}$ when Q_1 is switched "on" and Q_1 will conduct with a high on-state voltage and dissipate extra conduction loss;

if C_{ext} is too big, then the operation of the converter in which it is used will be delayed longer at start-up, as implied by Fig. 3-13.

APPENDIX (5) EFFECTIVE AND ACTUAL VOLUME OF CORES

A5-1 INTRODUCTION

When the magnetic properties of cores are calculated, the effective parameters are used. In this respect, the core is substituted by an ideal toroid such that a coil wound on that toroid would give exactly the same electrical performance as a coil with the same number of turns placed on the original core [1].

The effective volume of cores, V_e, is given according to international standards [1] by:

$$V_e = l_e A_e \tag{A5-1}$$

where: V_e is the effective volume of the core [mm^3],

l_e is the effective magnetic length of the core [mm],

A_e is the effective cross-sectional area of the core [mm^2], and

$$l_e = \frac{C_1^{\,2}}{C_2}\,,\quad A_e = \frac{C_1}{C_2} \tag{A5-2}$$

where: C_1 is the core constant [mm^{-1}] and

C_2 is the core constant [mm^{-3}], and are given by:

$$C_1 = \Sigma\frac{l}{A}\,,\quad C_2 = \Sigma\frac{l}{A^2} \tag{A5-3}$$

From Eq's (A5-1) and (A5-2), V_e can be written as:

$$V_e = \frac{C_1^{\,3}}{C_2^{\,2}} \tag{A5-4}$$

Always the effective volume of cores is less than the actual volume, V_a, due to sharp corners that do not contribute to power transfer and only add weight and size to the core. Field intensity and flux density are considerably crowded around inside the corners and, as a result, these corners saturate quickly [2]. Therefore, there is always loss in the material composing the core due to these ineffective parts.

The material loss depends on the geometry and complexity of the core. For simple shapes, it was found that the ratio of the effective to actual volume ranges between (80-96) %. The following sections show how this ratio can be calculated for ring (toroid), U- and E-shape cores. The same principle can be applied to any other shape.

A5-2 EFFECTIVE AND ACTUAL CORE VOLUME

A5-2-1 Ring Cores of Rectangular Cross-Section with Sharp Corners

Fig. A5-1 shows a ring core with an internal radius, r_1, external radius, r_2, and thickness, h. According to [1], the effective volume can be found as follows:

$$l_e = \frac{C_1^{\,2}}{C_2} = \frac{\left(\frac{2\pi}{h\log_e \frac{r_2}{r_1}}\right)^2}{\frac{2\pi\left(\frac{1}{r_1}-\frac{1}{r_2}\right)}{h^2 \log_e^{\,3} \frac{r_2}{r_1}}} = \frac{\frac{4\pi^2}{h^2 \log_e^{\,2} \frac{r_2}{r_1}}}{\frac{2\pi\left(\frac{1}{r_1}-\frac{1}{r_2}\right)}{h^2 \log_e^{\,3} \frac{r_2}{r_1}}}$$

$$l_e = \frac{2\pi \log_e \frac{r_2}{r_1}}{\frac{1}{r_1} - \frac{1}{r_2}} = \frac{2\pi r_1 r_2 \log_e \frac{r_2}{r_1}}{r_2 - r_1} \tag{A5-5}$$

$$A_e = \frac{C_1}{C_2} = \frac{h \log_e{}^2 \frac{r_2}{r_1}}{\frac{1}{r_1} - \frac{1}{r_2}} = \frac{h \log_e{}^2 \frac{r_2}{r_1}}{r_2 - r_1} r_2 r_1 \tag{A5-6}$$

$$V_e = l_e A_e = \frac{2\pi h (r_1 r_2)^2}{(r_2 - r_1)^2} \log_e{}^3 \frac{r_2}{r_1} \tag{A5-7}$$

The actual volume of the ring core is:

$$V_a = (\pi r_2{}^2 - \pi r_1{}^2) h = \pi (r_2{}^2 - r_1{}^2) \tag{A5-8}$$

$$\frac{V_e}{V_a} = \frac{2\pi h (r_1 r_2)^2 \log_e{}^3 \frac{r_2}{r_1}}{(r_2 - r_1)^2 \pi h (r_2{}^2 - r_1{}^2)} = \frac{2 (r_1 r_2)^2 \log_e{}^3 \frac{r_2}{r_1}}{(r_2{}^2 - r_1{}^2)(r_2 - r_1)^2} \tag{A5-9}$$

Eq. (A5-9) shows that the volume ratio depends on r_1 and r_2. Table A5-1 shows the volume ratios for three sizes of ring cores [3].

Core type	r_1 [mm]	r_2 [mm]	V_e/V_a [%]
RCC 20/7	4.7	10.25	86
RCC 31.5/12.5	9.15	16.05	92.5
RCL 58/17.5	20.25	29.35	96.6

Table A5-1 Volume ratios for different ring core sizes

From Table A5-1 we see that as the size of the ring core increases, the effective volume approaches the actual one. The physical interpretation of this is that as the core size increases, the curved shape of the core approaches a straight line, and the effective length and area, and hence the effective volume, approaches the actual ones.

A5-2-2 U-Core of Rectangular Section and Symmetrical Limbs

First, the individual lengths and areas for U-cores are defined, as shown in Fig. A5-2a and b.

$$l_1 = l_3 = 2B,\ l_2 = 2D,\ l_4 = l_5 = \frac{\pi}{4}(p+h),$$

$$A_1 = A_3 = pq,\ A_2 = qh,\ A_4 = A_5 = \frac{A_1 + A_2}{2} = \frac{q(p+h)}{2}$$

From Eq's (A5-2), (A5-3) and (A5-4), the effective volume can be found:

$$V_e = \frac{C_1^3}{C_2^2} = \frac{[2\frac{2B}{pq} + \frac{2D}{qh} + \frac{2\pi}{4}\frac{p+h}{q(\frac{p+h}{2})}]^3}{[\frac{4\pi}{(pq)^2} + \frac{2D}{(qh)^2} + \frac{2\pi}{4}\frac{p+h}{q^2\frac{(p+h)^2}{4}}]^2}$$

$$V_e = \frac{2q(\frac{2B}{p} + \frac{D}{h} + \frac{\pi}{2})^3}{[\frac{2B}{p^2} + \frac{D}{h^2} + \frac{\pi}{p+h}]^2} \qquad \text{(A5-10)}$$

The actual volume of U-cores can be given by:

$$V_a = 2[A(B+h)q - BDq]$$

$$V_a = 2q[A(B+h) - BD] \qquad \text{(A5-11)}$$

$$\frac{V_e}{V_a} = \frac{[\frac{2B}{q} + \frac{D}{h} + \frac{\pi}{2}]^3}{[A(B+h) - BD][\frac{2B}{p^2} + \frac{D}{h^2} + \frac{\pi}{p+q}]^2} \qquad \text{(A5-12)}$$

Table A5-2 shows the volume ratio for four U-core sizes [3].

Core type	A [mm]	B [mm]	D [mm]	h [mm]	p [mm]	q [mm]	V_e/V_a %
U100/57/25	101.6	31.7	50.8	25.4	25.4	25.4	93.5
U93/76/30	93	48	37	26	28	30	93.7
U93/52/30	93	24	37	28	28	30	91.4
U30/25/16	32	14.5	12.3	11	9.85	16.25	92.2

Table A5-2 Volume ratio for different U-core sizes

A5-2-3 E-core of rectangular cross-section

First, the individual lengths and areas for E-cores, as shown in Fig. A5-3a and b, are defined:

$$l_1 = l_3 = B,\ l_2 = D,\ l_4 = \frac{\pi}{8}(p+h),\ l_5 = \frac{\pi}{8}(s+h)$$

$$A_1 = pq,\ A_2 = qh,\ A_3 = qs,\ A_4 = \frac{A_1 + A_2}{2} = \frac{q(p+h)}{2},\ A_5 = \frac{A_2 + A_3}{2} = \frac{q(s+h)}{2}$$

$$V_e = \frac{C_1^3}{C_2^2} = \frac{[\frac{B}{pq} + \frac{D}{qh} + \frac{B}{qs} + \frac{2\pi}{8}\frac{p+h}{q(p+h)} + \frac{2\pi}{8}\frac{s+h}{q(s+h)}]^3}{[\frac{B}{2(pq)^2} + \frac{D}{2(qh)^2} + \frac{B}{2(qs)^2} + \frac{4\pi}{8}\frac{p+h}{2q^2(p+h)^2} + \frac{4\pi}{8}\frac{s+h}{2q^2(s+h)^2}]^2}$$

$$V_e = \frac{4q[\frac{B}{p}+\frac{D}{h}+\frac{B}{s}+\frac{\pi}{2}]^3}{[\frac{B}{p^2}+\frac{D}{h^2}+\frac{B}{s^2}+\frac{\pi}{2(p+h)}+\frac{\pi}{2(s+h)}]^2} \quad \text{(A5-13)}$$

The actual volume of U-cores is:

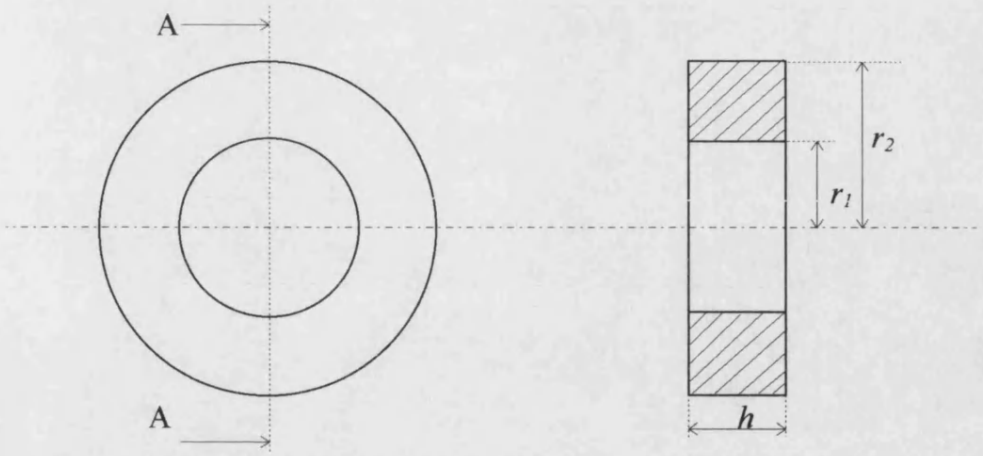
$$V_a = 4[\frac{A}{2}(B+h)q - BDq] = 4q[\frac{A}{2}(B+h) - BD] \quad \text{(A5-14)}$$

$$\frac{V_e}{V_a} = \frac{[\frac{B}{p}+\frac{D}{h}+\frac{B}{s}+\frac{\pi}{2}]^3}{[\frac{A}{2}(B+h) - BD][\frac{B}{p^2}+\frac{D}{h^2}+\frac{B}{s^2}+\frac{\pi}{2(p+h)}+\frac{\pi}{2(s+h)}]^2} \quad \text{(A5-15)}$$

Table A5-3 shows the volume ratio for three sizes of E-cores [3].

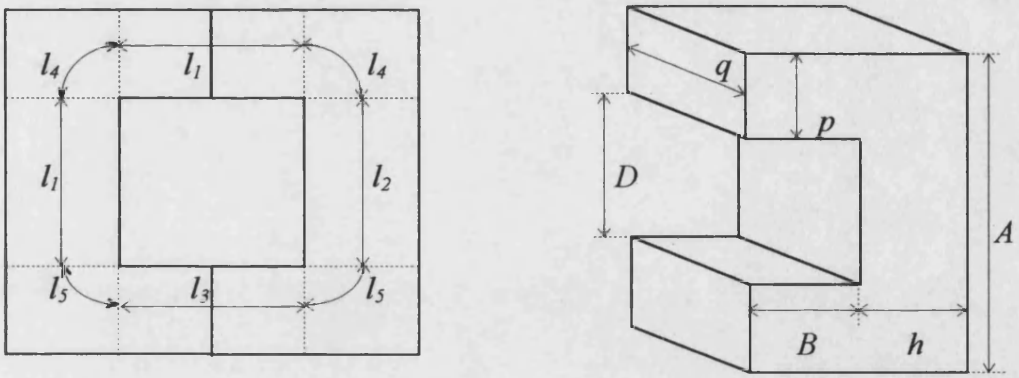
Core type	A [mm]	B [mm]	D [mm]	p [mm]	h [mm]	s [mm]	q [mm]	V_e/V_a [%]
E65/32/27	65	22.2	11.1	10.4	10.6	10	27.4	90.2
E47/20/16	46.9	12.4	8.4	7.25	7.2	7.8	15.6	93.2
E30/15/13	30.8	9.7	6.15	5.65	5.5	3.6	12.6	83.3

Table A5-3 Volume ratios for different E-core sizes



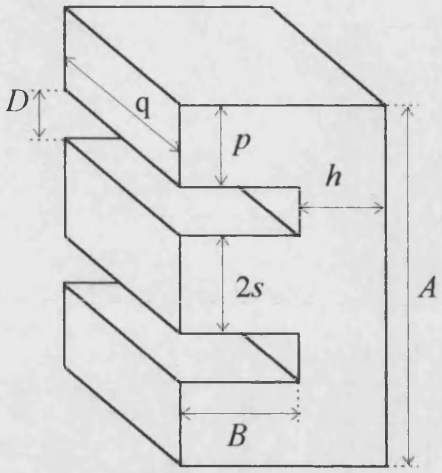
a) Top view b) Section A-A

Fig. A5-1 A ring core of rectangular cross-section

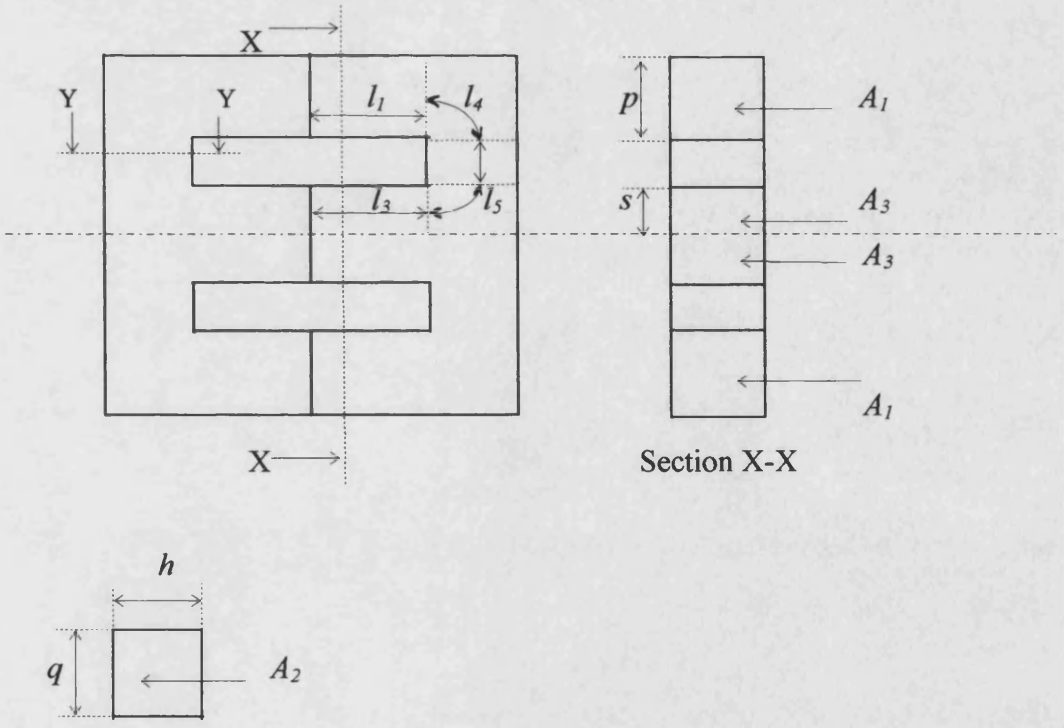


a) Cross section b) General view

Fig. A5-2 A U-core of rectangular section and symmetrical limbs



a) General view



b) Cross-section

Fig. A5-3 An E-core of rectangular cross-section

REFERENCES

1. British Standard BS 6454 : 1983, British Standard method for calculation of the effective parameters of magnetic piece parts, British Standard Institution, p.p. 1172-1191, 1983.
2. Lloyd Dixon, "An electrical circuit model for magnetic cores", Power Supply Design Seminar, SEM1000, Unitrode, 1994, p.p. 6-1 to 6-9.
3. Soft Ferrites, Book MA01, Philips, 1993.

APPENDIX SIX

Design Equations for Flyback Inverters

$$T_{R(\max)} = \frac{L_S \hat{I}_S}{\hat{V}_O} = \frac{L_S}{\hat{V}_O}\frac{N_P}{N_S}\hat{I}_P = \frac{L_S}{\hat{V}_O}\frac{N_P}{N_S}\frac{V_{DC(\min)} T_{ON(\max)}}{L_P} \quad \text{(A6-1)}$$

$$T_{R(\max)} = \frac{N_S}{N_P}\frac{V_{DC(\min)}}{\hat{V}_O} T_{ON(\max)} \quad \text{(A6-2)}$$

$$T_S = T_{R(\max)} + T_{ON(\max)} + kT_S \Rightarrow T_{R(\max)} = (1-k)T_S - T_{ON(\max)} \quad \text{(A6-3)}$$

where $T_{R(\max)}$ is the maximum reset time, T_S is the switching period, L_P is the primary winding inductance and k is a fraction to ensure that the secondary current is reset each switching period and may be assumed 0.2.

Combining Eq's (A6-1) and (A6-2) gives:

$$(1-k)T_S - T_{ON(\max)} = \frac{N_S}{N_P}\frac{V_{DC(\min)}}{\hat{V}_O} T_{ON(\max)} \Rightarrow$$

$$T_{ON(\max)} = \frac{(1-k)T_S}{1 + N\dfrac{V_{DC(\min)}}{\hat{V}_O}} \quad \text{(A6-4)}$$

where $N = \dfrac{N_S}{N_P}$ is the transformer turns ratio.

The instantaneous primary peak current at the end of each switching cycle is:

$$\hat{i}_P = \frac{V_{DC} T_{ON}}{L_P} = \frac{V_{DC} T_{ON(\max)}}{L_P} \sin \omega t \quad \text{(A6-5)}$$

The maximum primary peak current:

$$\hat{I}_P = \frac{V_{DC(\min)} T_{ON(\max)}}{L_P} = \frac{V_{DC(\min)} (1-k) T_S}{L_P (1 + N \frac{V_{DC(\min)}}{\hat{V}_O})} \tag{A6-6}$$

To find L_P, a formula for the input power may be written in terms of the output power and efficiency as follows:

$$P_{IN} = \frac{P_O}{\eta} \tag{A6-7}$$

Also, the input power may be written in terms of the input energy as follows:

$$P_{IN} = \frac{1}{\pi} \sum_{0}^{\pi} \frac{\frac{1}{2} L_P \hat{i}_P^{\,2}}{T_S} = \frac{L_P}{2\pi T_S} \int_0^{\pi} [\frac{V_{DC(\min)} T_{ON(\max)}}{L_P} \sin\theta]^2 d\theta \tag{A6-8}$$

$$P_{IN} = \frac{[V_{DC(\min)} T_{ON(\max)}]^2}{4 T_S L_P} \tag{A6-9}$$

Combining Eq's (A6-7) and (A6-9) gives:

$$L_P = \frac{\eta [V_{DC(\min)} T_{ON(\max)}]^2}{4 T_S P_O} = \frac{\eta (1-k)^2 T_S}{4 P_O (\frac{1}{V_{DC(\min)}} + \frac{N}{\hat{V}_O})^2} \tag{A6-10}$$

APPENDIX SEVEN

A7-1 Estimating Voltage-Rise and Current-Fall Times is Switching Circuits

The turn-off energy loss during each switching cycle may be given by Eq. (A7-1) if the voltage rise time, T_{VR}, and the current fall time, T_{CF}, are theoretically calculated as shown in Fig. A7-1a. If both times are measured at 10% of the final value, as shown in Fig. A7-1b, then Eq. (A7-2) is applied. If each time is measured from 10% to 90%, as shown in Fig. A7-1c, then Eq. (A7-3) is applied.

$$W_{Q(off)} = \frac{1}{2} VI(\theta)(T_{VR} + T_{CF}) \tag{A7-1}$$

$$W_{Q(off)} = \frac{1.1}{2} VI(\theta)(T_{VR} + T_{CF}) \tag{A7-2}$$

$$W_{Q(off)} = \frac{1.2}{2} VI(\theta)(T_{VR} + T_{CF}) \tag{A7-3}$$

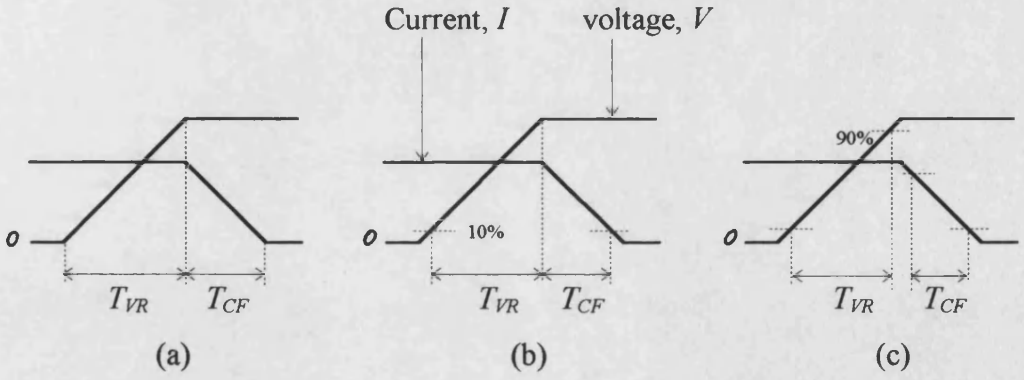
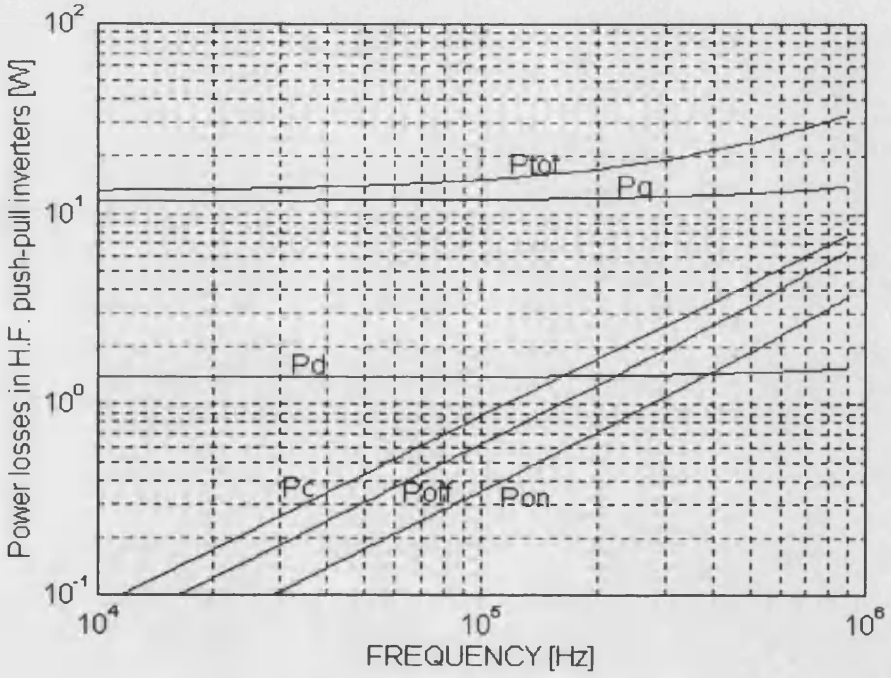


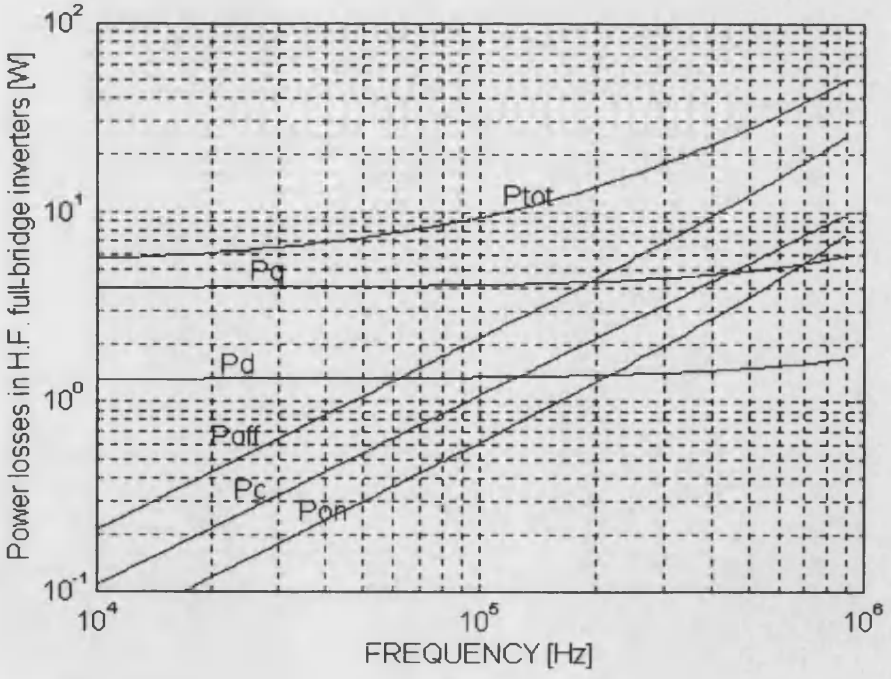
Fig. A7-1 Definitions of voltage-rise and current-fall times, a) calculated, b) measured at 10% and c) measured from 10% to 90%

Topology	P_O [W]	$V_{DC(min)}$ [V]	r_Q [Ω]	r_D [Ω]	V_{DO} [V]	m_a [-]	N [-]	Q_{RRR} [nc]	I_{DR} [A]	di/dt [A/μs]	T_{VR} [ns]	C_{OSS} [pF]	ϕ [rad]
L.F. Push-pull	200	125	1.5	0.1	0.5	0.8	1	2	3.1	100	8	60	0.45
L.F. Half-Bridge	"	"	0.4	"	"	"	2	2.2	5.9	"	35	150	"
L.F. Full-Bridge	"	"	"	"	"	"	1	"	"	"	"	"	"
H.F. S-E Forward	"	"	0.85	"	"	0.4	2	4.2	8	"	11.5	125	"
H.F. D-E Forward	"	"	0.4	"	"	"	2	2.2	5.9	"	35	150	"
H.F. Push-Pull	"	"	1.5	"	"	0.8	1	2	3.1	"	8	60	"
H.F. Half-Bridge	"	"	0.4	"	"	"	2	2.2	5.9	"	35	150	"
H.F. Full-Bridge	"	"	"	"	"	"	1	"	"	"	"	"	"

A7-2 Parameter values used to estimate switching and conduction power-loss in dc/ac inverter topologies



(a)



(b)

Fig. A7-2 Power losses versus frequency for high-frequency a) push-pull and b) full-bridge inverters at maximum d.c. supply voltage (compare with Fig's 7-2f and h)

A7-4 A MATLAB Program to Estimate and Draw Switching and Conduction Power Losses in the High-Frequency Full-Bridge Inverter Given in Ch. 7

```
vmin=125; ma=0.8; eff=0.8; coss=150e-12; po=200; fai=0.45; rd=0.1; rqp=0.4;
rqs=0.4; vqpo=0; vqso=0; vdo=0.5; qrrr=2.2e-9; idr=5.9; di=1e8; tvr=35e-9; n=1;
eata8=[]; pt8=[]; pq8=[]; pd8=[]; pof8=[]; pon8=[]; fs8=[]; pc8=[];

for x=4:5
  for y=1:0.2:9
    fsw=y*10^x;
    i=0;
    while i==0
      n=ns/np;                                          % turns ratio
      ip=2*po/(eff*ma*vmin*cos(fai));                   % peak primary current
      tcf=ip/di;                                        % maximum current fall time
      pqc=vqpo*ip*ma*cos(fai)+8*ma*rqp*ip^2*cos(fai)/(3*pi)+
      2*vqso*ip/(pi*n)+rqs*ip^2/(2*n^2);                % switches cond power loss
      pdc=2*vdo*ip/(pi*n)+2*rd*ip^2*ma*
      cos(fai)/(3*n^2*pi)+rd*ip^2/(4*n^2);              % diode cond power loss
      poff=fsw*vmin*ip*(4*tvr+pi*tcf)/(2*pi);           % turn-off power loss
      ponn=fsw*vmin*(2*ip*qrrr/idr+2.472*ip*
     (qrrr*ip/(idr*di))^0.5+pi*ip^2/(4*di))/pi;         % turn-on power loss
      pcoss=2*fsw*coss*vmin^2;                          % Coss power loss
      p=po/(po+pqc+pdc+poff+ponn+pcoss);
      if abs(p-eff)>0.001                               % efficiency tolerance 0.1%
        eff=p;
        else i=1;
      end
    end
    eata8=[eata8;eff];
    pq8=[pq8;pqc];
    pd8=[pd8;pdc];
    pof8=[pof8;poff];
    pon8=[pon8;ponn];
    pc8=[pc8;pcoss];
    ptot=pqc+pdc+poff+ponn+pcoss;
    pt8=[pt8;ptot];
    fs8=[fs8;fsw];
  end
end
loglog(fs8,pof8,'w',fs8,pon8,'w',fs8,pq8,'w',fs8,pd8,'w',fs8,pt8,'w',fs8,pc8,'w')
%loglog(fs8,pt8,'w')
%loglog(fs8,eata8,'w')
grid
axis([1e4 1e6 1e-1 1e2])
end
```

APPENDIX NINE

Axiale Elektrolyt - Kondensatoren gepolte Ausführung, rauhe Elektroden, schaltfest, DIN 41316 u. 45910, Teil 126

EL, EB, EG

Technische Angaben:

Abnahmereststrom

$I_{ra} \leqq 0{,}0015 \cdot C_R \cdot U_R + 2\ \mu A$ (C_R in µF, U_R in V–) für ≦ 100 V–

$I_{ra} \leqq 0{,}015 \cdot C_R \cdot U_R + 10\ \mu A$ (C_R in µF, U_R in V–) für > 100 V–

Abm.: 3,2 x 11 u. 4,5 x 11 (3,5x 7): $I_{ra} \leqq 0{,}002 \cdot C_R \cdot U_R + 5\ \mu A$ (C_R in µF, U_R in V–) für ≦ 100 V–

gemessen an U_R bei 20°C nach 5 Min.

Abnahmereststrom siehe auch unter „Allgemeine Angaben".

Verlustfaktor (Größtwerte)

U_R	6,3	10	16	25	40	50	63	100	160	250	350	385	V –
tan δ	0,15	0,12	0,10	0,08	0,07	0,06	0,05	0,04	0,04	0,04	0,04	0,06	50 Hz
tan δ	0,25	0,20	0,16	0,14	0,12	0,10	0,08	0,07	0,07	0,07	0,07	0,10	100 Hz

gemessen mit 0,5 V_{eff} bei 20°C.

Bei Kap.-Werten über 1000 µF erhöhen sich obige 50 Hz- / 100 Hz-Werte um 0,01 / 0,02 je 1000 µF.
Für die Becherdurchmesser 3,2 (3,5) und 4,5 mm gelten die tan δ-Werte nach DIN 41332.

Ersatzserienwiderstand R_{ESR} in Ω · µF (Größtwerte) $R_{ESR} = \frac{\text{Tabellenwert}}{C_R}$

U_R	6,3	10	16	25	40	50	63	100	160	250	350	385	V –
Ω · µF	480	380	320	260	225	190	160	130	130	130	130	190	50 Hz
Ω · µF	400	320	260	220	190	160	130	110	110	110	110	160	100 Hz

bei 20°C; bezogen auf 1 µF.

Bei Kap.-Werten über 1000 µF erhöhen sich obige 50 Hz- / 100 Hz-Werte um 32 Ω · µF je 1000 µF.

Scheinwiderstand (Z) in Ω · µF (Größtwerte) $Z = \frac{\text{Tabellenwert}}{C_R}$

U_R	1 kHz/20°C	1 kHz/–25°C	1 kHz/–40°C	10 kHz/20°C	10 kHz/–25°C	10 kHz/–40°C
(V)	(Ω · µF)	(Ω · µF)	(Ω · µF)	(Ω · µF)	(Ω · µF)	(Ω · µF)
6,3	390	1 900	5 000	220	1 300	4 800
10	330	1 200	3 100	160	1 000	3 500
16	280	880	2 200	130	860	2 400
25	240	630	1 500	90	440	1 200
40	220	470	1 200	75	330	990
50	210	420	1 060	65	270	800
63	195	360	880	55	200	550
100	190	330	770	45	160	500
[illegible]	180	600	2 500	120	1 000	5 000
[illegible]	190	1 000	10 000	110	1 000	4 600
[illegible]	210	3 400	14 500	100	1 500	4 600
385	380	17 000	18 000	100	1 800	6 000

Der praktisch erreichbare Serien- und Scheinwiderstand ist durch den ohmschen Anteil der Kontaktverbindungen und der Folienwiderstände nach unten begrenzt. Daher sind errechnete Werte unter 0,05 Ω nicht in jedem Fall zu realisieren.

[illegible] Wechselstrombelastbarkeit in Abhängigkeit von der Umgebungstemperatur sowie Frequenzabhängigkeit des [illegible] siehe unter „Allgemeine Angaben"

APPENDIX ELEVEN

H [Oe]	0	0.187	0.4	0.6	0.8	1	1.5
B_U[mT]	111.2	200.5	262.1	303.6	332.2	354.1	391.5
B_L[mT]	-111.2	0	103.5	183.4	240.6	283.8	352.9

H [Oe]	2	2.5	3	4	5	6	7
B_U[mT]	415.6	432.2	444.1	460.6	471.4	479	484.7
B_L[mT]	392.3	416.6	432.9	453.9	466.9	475.8	482.3

H [Oe]	8	9	10	11	9	14	15
B_U[mT]	489.1	492.6	495.5	497.9	500	503.3	504.6
B_L[mT]	487.2	491.1	494.3	496.9	499.1	502.6	504.1

App. (11) Major hysteresis loop values as taken from PSPICE V 6.1

APPENDIX 12-1

MAPLE PROGRAM TO SOLVE EQUATIONS (12-6) AND (12-8)

```
> Ls=a*Lm:

> Rs=b*RL:

> de1 :=a*Lm*diff(IS(t),t)-Vs+IS(t)*b*RL+(IS(t)-IM(t))*RL=0:

> de2 :=Lm*diff(IM(t),t)-(IS(t)-IM(t))*RL=0:

> sys :={de1,de2,IS(0)=0,IM(0)=0};
```

INPUT FILE

$$sys := \left\{ a\,Lm\left(\frac{\partial}{\partial t}\mathrm{IS}(t)\right) - Vs + \mathrm{IS}(t)\,b\,RL + (\mathrm{IS}(t) - \mathrm{IM}(t))\,RL = 0,\ Lm\left(\frac{\partial}{\partial t}\mathrm{IM}(t)\right) - (\mathrm{IS}(t) - \mathrm{IM}(t))\,RL = 0,\ \mathrm{IS}(0) = 0,\ \mathrm{IM}(0) = 0 \right\}$$

OUTPUT FILE

```
fcns:={IS(t),IM(t)};

dsolve(sys, fcns);
```

INPUT FILE

$$fcns := \{\mathrm{IM}(t), \mathrm{IS}(t)\}$$

OUTPUT FILE

$$
\left\{
\begin{aligned}
&\mathrm{IM}(t) = -4\,a\left(-\frac{1}{4} Vs \left(1 + \sqrt{\%1} - \sqrt{\%1}\, b + \sqrt{\%1}\, a \right.\right. \\
&\quad - 2\,b\,a + b^2 + 2\,b + 2\,a + a^2\big)\big(\sqrt{\%1}\, b + \sqrt{\%1} \\
&\quad - \sqrt{\%1}\, a + b^2 + 2\,b - 2\,b\,a + 1 + 2\,a + a^2\big) \\
&\quad \mathrm{e}^{\left(1/2 \frac{RL\left(-b-1-a+\sqrt{\%1}\right)t}{Lm\,a}\right)} / \%1^{3/2} + \frac{1}{4} Vs \left(1 - \sqrt{\%1}\right. \\
&\quad + \sqrt{\%1}\, b - \sqrt{\%1}\, a - 2\,b\,a + b^2 + 2\,b + 2\,a + a^2\big)\big(\\
&\quad -2\,b\,a + a^2 + b^2 + \sqrt{\%1}\, a - \sqrt{\%1}\, b - \sqrt{\%1} + 1 + 2\,b \\
&\quad \left. + 2\,a\right) \mathrm{e}^{\left(-1/2 \frac{RL\left(b+1+a+\sqrt{\%1}\right)t}{Lm\,a}\right)} / \%1^{3/2} + Vs \Big) / (RL \\
&\quad \left(-b - 1 - a + \sqrt{\%1}\right)\left(b + 1 + a + \sqrt{\%1}\right)\big), \mathrm{IS}(t) = -4\,a\Big(\\
&\quad -\frac{1}{2} Vs \left(1 + \sqrt{\%1} - \sqrt{\%1}\, b + \sqrt{\%1}\, a - 2\,b\,a + b^2 + 2\,b \right. \\
&\quad \left. + 2\,a + a^2\right) \mathrm{e}^{\left(1/2 \frac{RL\left(-b-1-a+\sqrt{\%1}\right)t}{Lm\,a}\right)} / (\%1) - \frac{1}{2} Vs \left(1 \right. \\
&\quad - \sqrt{\%1} + \sqrt{\%1}\, b - \sqrt{\%1}\, a - 2\,b\,a + b^2 + 2\,b + 2\,a + a^2 \\
&\quad \left. \right) \mathrm{e}^{\left(-1/2 \frac{RL\left(b+1+a+\sqrt{\%1}\right)t}{Lm\,a}\right)} / (\%1) + Vs \Big) / (RL \\
&\quad \left.\left(-b - 1 - a + \sqrt{\%1}\right)\left(b + 1 + a + \sqrt{\%1}\right)\right)\Big\}
\end{aligned}
\right\} \text{OUTPUT FILE}
$$

$$
\%1 := b^2 + 2\,b - 2\,b\,a + 1 + 2\,a + a^2
$$

APPENDIX 12-2

```
% plots variations in time constant multipliers for transformer model
% Ls=a*Lm and Rs=b*RL
% z=1+2a+2b+a^2-2ab+b^2
% Tau1=2aLm/(RL(1+a+b+z^.5))
% Tau2=2aLm/(RL(1+a+b-z^.5))
clear all
a=logspace(-4,3,100)
        b=1+0*a;
        z=1+2*(a+b)+(a-b).^2;
        x1=2*a./(1+a+b+z.^.5);
        x2=2*a./(1+a+b-z.^.5);
        y1=(b+1)./b;
        y2=a./(1+b);
loglog(a,x1,'r',a,x2,'g',a,y1,'--',a,y2,'--')
grid
title('variation in normalised time-constant with a, where a=Ls/Lm')
xlabel('a=Ls/Lm')
ylabel('Time-constant normalised to Lm/RL')
end
hold on
        b=.0001+0*a;
        z=1+2*(a+b)+(a-b).^2;
        x1=2*a./(1+a+b+z.^.5);
        x2=2*a./(1+a+b-z.^.5);
        y1=(b+1)./b;
        y2=a./(1+b);
loglog(a,x1,'b',a,x2,'y',a,y1,'--',a,y2,'--')
hold off
end
```

APPENDIX 12-3

CALCULATING THE TIME CONSTANT FOR ESTIMATING THE TIME REQUIRED BY AN INDUCTOR OR A TRANSFORMER TO REACH STEADY-STATE FLUX CONDITIONS

Fig. A12-2 shows the initial magnetising current for the circuit of Fig. 12-4a, as taken from PSPICE using the following parameters:

$L_S = 0$, $R_S = 5\ \Omega$, $N_P = 10$, $N_S = 4$, $R_L = 10\ g\Omega$, $A_e = 3.68\ cm^2$ and $l_e = 13.9$ cm.

The peak of the magnetising current starts at a high value, I_{MAX}, decreasing exponentially with a time constant τ to a steady-state value of I_{SS}. τ is the time taken by the magnetising current to reach $1/e$, or 0.368 of the current between I_{MAX} and I_{SS}, i.e. $0.368I_O$ in Fig. A12-1. Therefore, to find τ, the current at $t = \tau$, i.e. $i(t = \tau)$ should be calculated as follows:

$$i(t = \tau) = 0.368I_O + I_{SS}$$
$$i(t = \tau) = 0.368(I_{MAX} - I_{SS}) + I_{SS}$$
$$i(t = \tau) = 0.368I_{MAX} + 0.632I_{SS} \qquad \text{(A12-1)}$$

If we draw a horizontal line at $i(t=\tau)$, it crosses the envelop of the magnetising current at point τ. The distance from this point to the time origin is the time constant τ.

For Fig. A12-2 if we extend the envelop of the magnetising current to the time origin, we get $I_{MAX} \approx 1$ A. Since I_{SS} is 462 mA, as seen from the figure, then $i(t = \tau) = 660$ mA. Drawing a horizontal line at 660 mA gives $\tau = .22$ ms.

One source of errors of this method is how to obtain I_{MAX}. Another way of finding τ without having to find I_{MAX} is as follows:

Fig. A12-1 shows the envelop of a similar current waveform, from which we can write, after ignoring the offset value I_{SS}:

$$i(t_1) = I_O e^{-t_1/\tau} \tag{A12-2}$$

$$i(t_2) = I_O e^{-t_2/\tau} \tag{A12-3}$$

Eliminating I_O from Eq's (A12-2) and (A12-3) gives:

$$\frac{i(t_1)}{i(t_2)} = \frac{e^{-t_1/\tau}}{e^{-t_2/\tau}} = e^{(t_2-t_1)/\tau} \tag{A12-4}$$

Taking the natural logarithm of both sides of Eq. (A12-4) gives:

$$Ln\frac{i(t_1)}{i(t_2)} = (t_2 - t_1)/\tau \tag{A12-5}$$

which gives:

$$\tau = \frac{t_2 - t_1}{Ln\dfrac{i(t_1)}{i(t_2)}} \tag{A12-6}$$

Therefore, it is possible to calculate τ using Eq. (A12-6) by taking two current values at two different time instants. This method predicts the time constant of any system provided that time constant does not vary with time. In fact, in the simulated circuit, as time increases, the magnetising inductance, L_M, changes and the time constant also changes since it is proportional to L_M. The maximum time constant can be found at the time origin where L_M is high. For Fig. A12-2, time constants of (0.2-0.36) ms were found within the time range (0-0.5) ms.

How τ can be calculated analytically:

As described in Sec. (12-2-1), the time constant of the circuit of Fig. 12-4 may be approximated at low a values by $\tau = L_M/R_S$. R_S is given in the application, while L_M can be calculated from the following formula:

$$L_M = \frac{A_e}{l_e} N_P^{\,2} \mu_o \mu_r \qquad \text{(A12-7)}$$

All parameters in Eq. (A12-7) are constant for each design except μ_r, which is a variable non-linear parameter with the flux density, B. Fig. A12-3 shows how μ_r varies during the simulation of Fig. 12-4, where we used the expression dB/dH to describe μ_r. From Fig. A12-3 we see that at the beginning of the simulation, μ_r excursion around its average value is high and equals about 3000. At about 0.22 ms, the average value of μ_r decreases to about 2700. Therefore, the average of the two averages was taken for the time constant calculations, i.e.

$$\mu_r = (3000+2700)/2=2850$$

is the value used in Eq. A12-7 to calculate L_M, from which the time constant τ was found as described in Sec. (12-2-1).

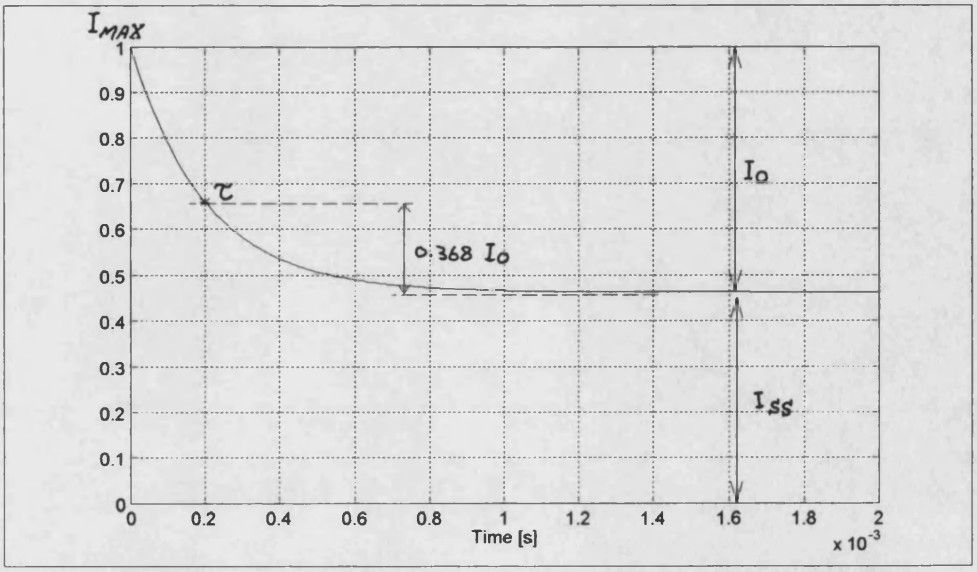


Fig. A12-1 A graph to show how the time constant can be calculated

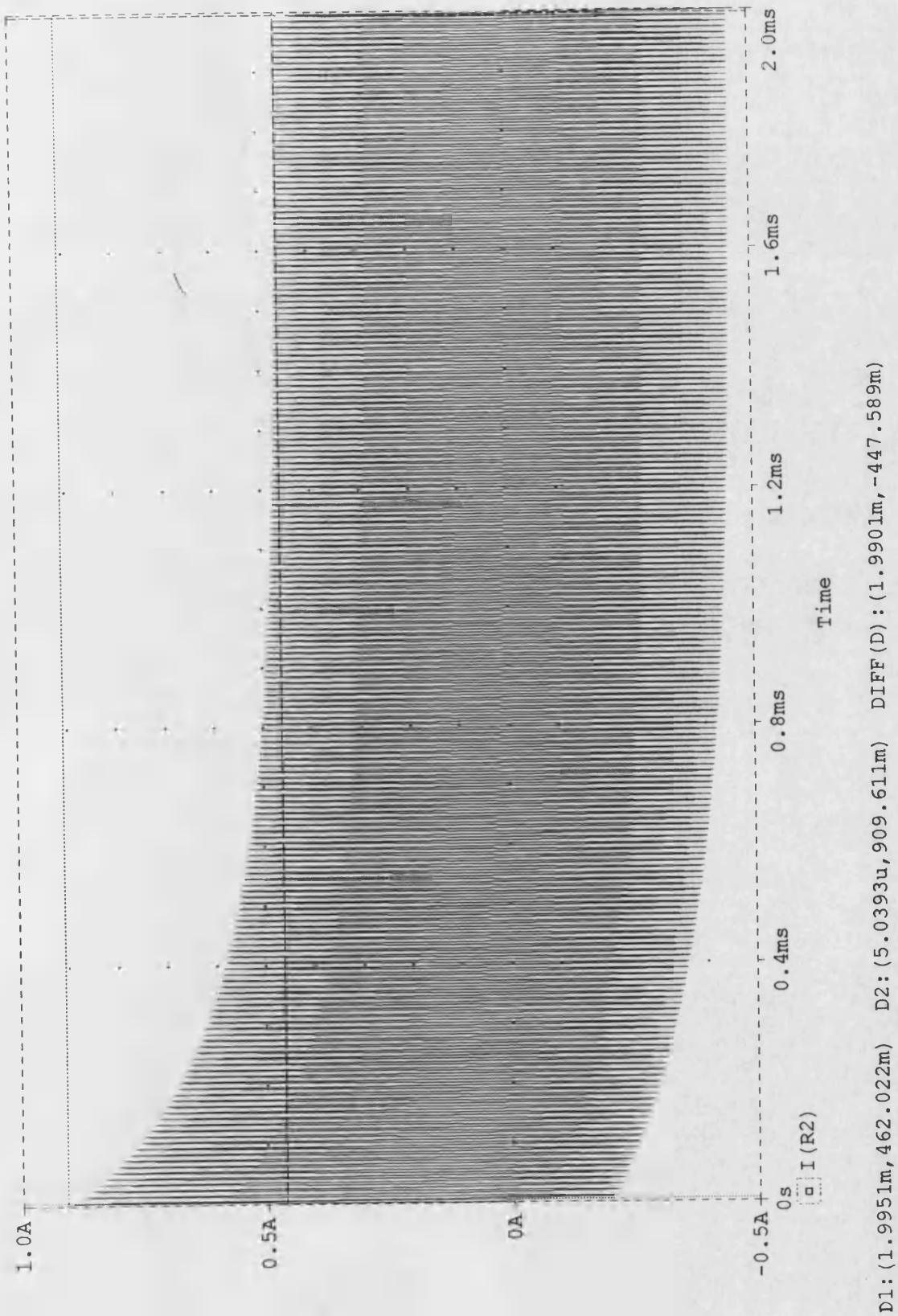


Fig. A12-2 The initial values of the magnetising current

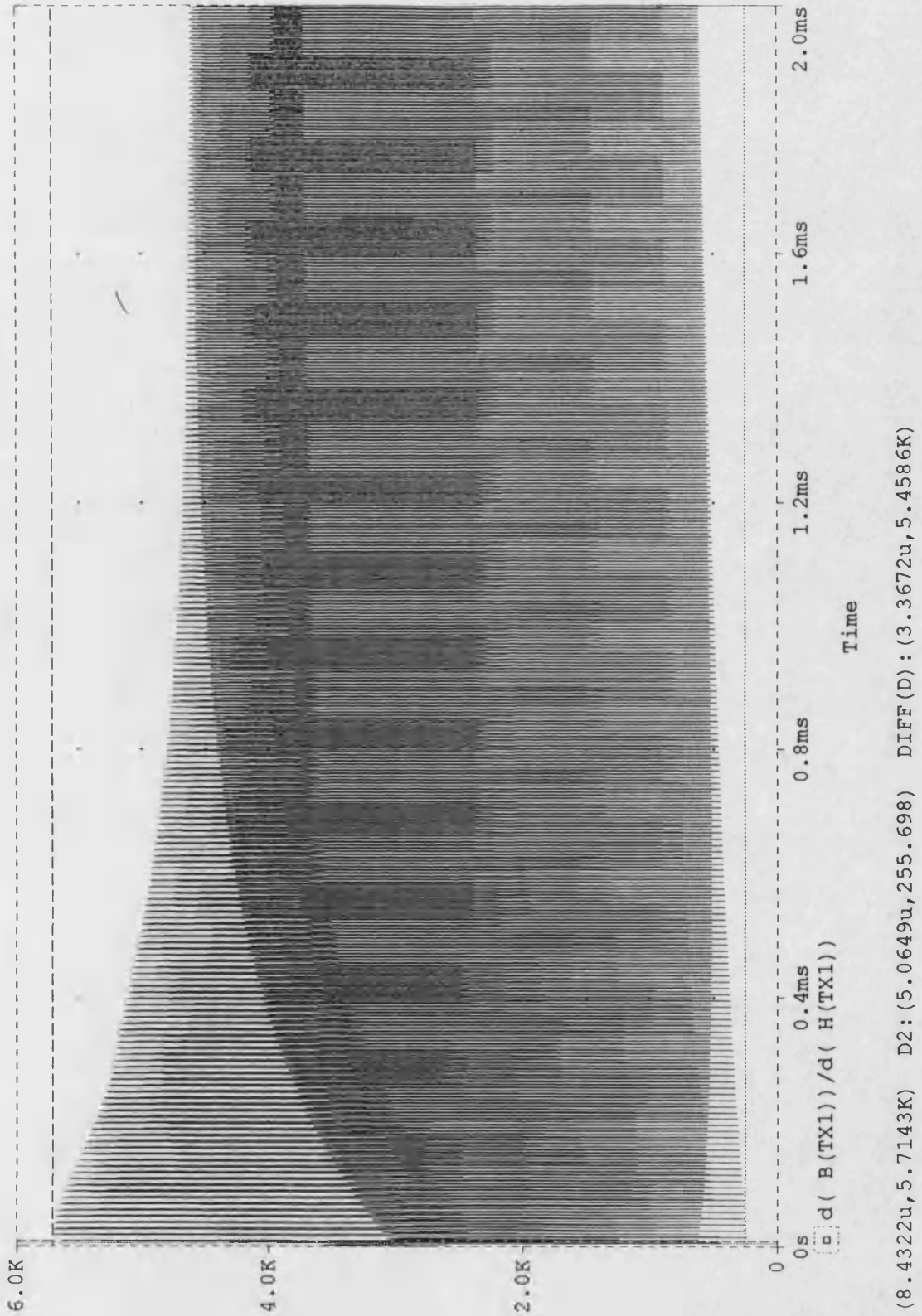


Fig. A12-3 μ_r variations of Fig. A12-2 during simulation

APPENDIX 12-4

B (mT)	0	25	50	75	100	117	133	150
μ_r	3408	3768	4085	4373	4599	4736	4824	4877

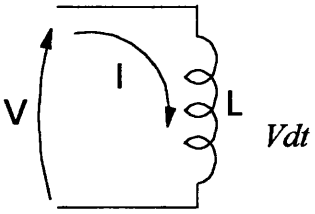
B (mT)	167	175	183	200	217	225	233	250
μ_r	4901	4908	4894	4824	4718	4627	4525	4268

B (mT)	267	275	283	300	325	350	358	400
μ_r	3930	3680	3472	2905	1796	528	1	1

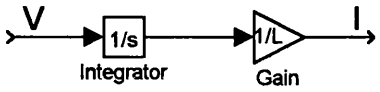
App. (12-4) Look-up table parameters for the relation between μ_r and B for 3C85 grade [4]

APPENDIX 12-5

SOME LOAD CONFIGURATIONS, THE EQUATIONS RELATING IL TO VS, AND HOW IT CAN BE IMPLEMENTED IN MATLAB

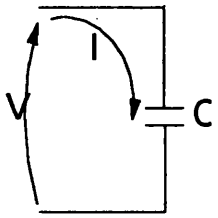


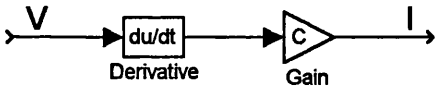
$$I = \frac{1}{L}\int Vdt$$



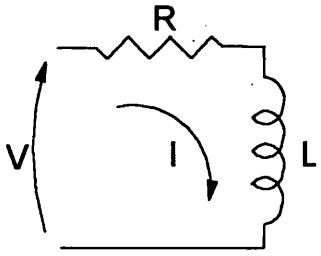
.....

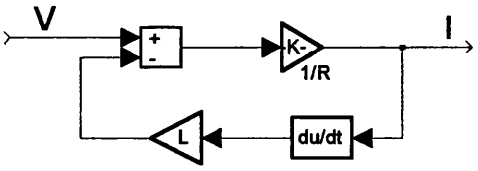
$$I = C\frac{dV}{dt}$$





.....

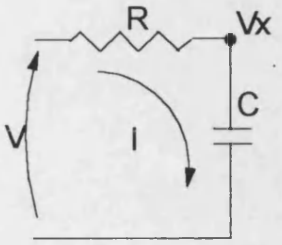




$$V = RI + L\frac{dI}{dt}$$

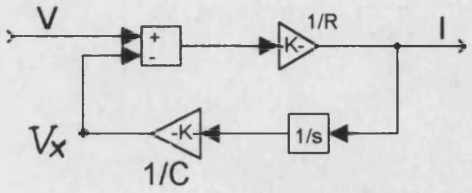
$$I = \frac{1}{R}(V - L\frac{dI}{dt})$$

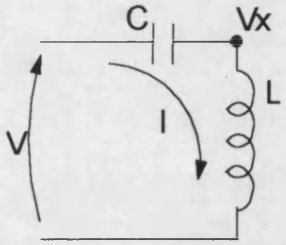
.....



$$I = \frac{V - Vx}{R}$$

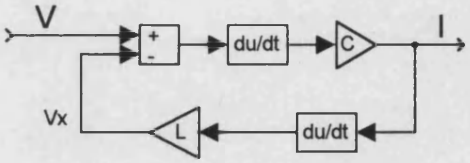
$$Vx = \frac{1}{C}\int Idt$$

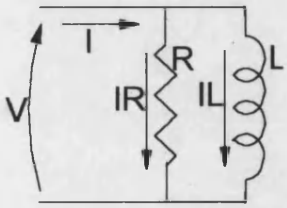


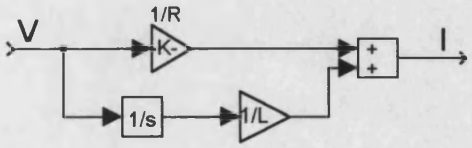


$$I = C\frac{d(V - Vx)}{dt}$$

$$Vx = L\frac{dI}{dt}$$

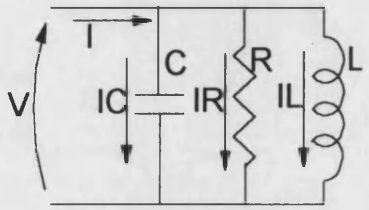


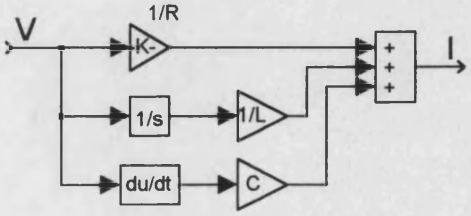




$$I = I_R + I_L$$

$$I = \frac{V}{R} + \frac{1}{L}\int Vdt$$

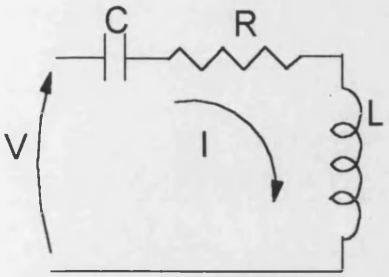


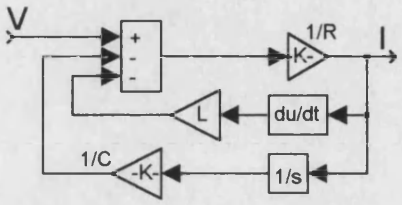


$$I = I_R + I_L + I_C$$

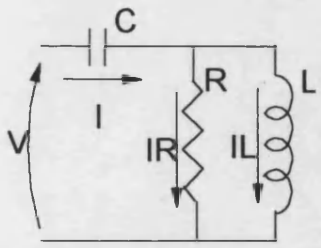
$$I = \frac{V}{R} + C\frac{dV}{dt} + \frac{1}{L}\int Vdt$$

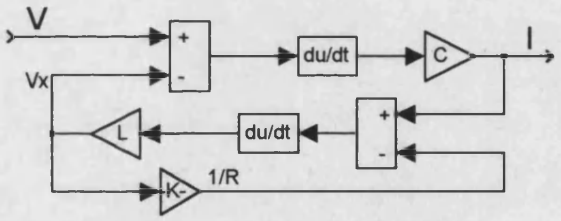
$$V = RI + L\frac{dI}{dt} + \frac{1}{C}\int Idt \quad , \qquad I = \frac{1}{R}(V - L\frac{dI}{dt} - \frac{1}{C}\int Idt)$$



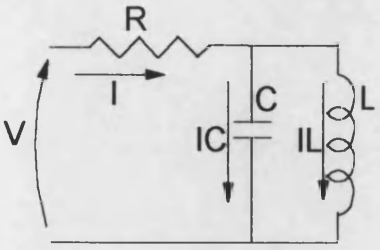


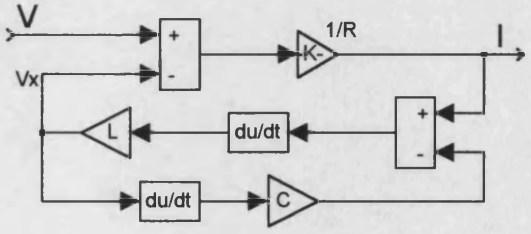
$$I = C\frac{d(V - Vx)}{dt}, Vx = L\frac{dI_L}{dt}, \; I_L = I - I_R \; , \; I_R = \frac{Vx}{R}$$





$$I = \frac{V - Vx}{R} \; , \; Vx = L\frac{dI_L}{dt} \; , I_L = I - I_C \; , \; I_C = C\frac{dVx}{dt}$$





APPENDIX 14-1

A MATLAB PROGRAM TO DRAW FIG. 14-11

```
%normalised material saving in three-limb core-type arrangements
clear all
k=linspace(0,10,100);
x=(3*k-2)./(6*(k+1));
plot(k,x,'r')
hold on
plot(5/6,.045,'*',8/3,.273,'*',2.5,.262,'*',1.6,.18,'*')
grid
xlabel('k')
ylabel('Normalised material saving')
hold off
gtext('1');
gtext('2');
gtext('3');
gtext('4');
end
```

APPENDIX 14-2

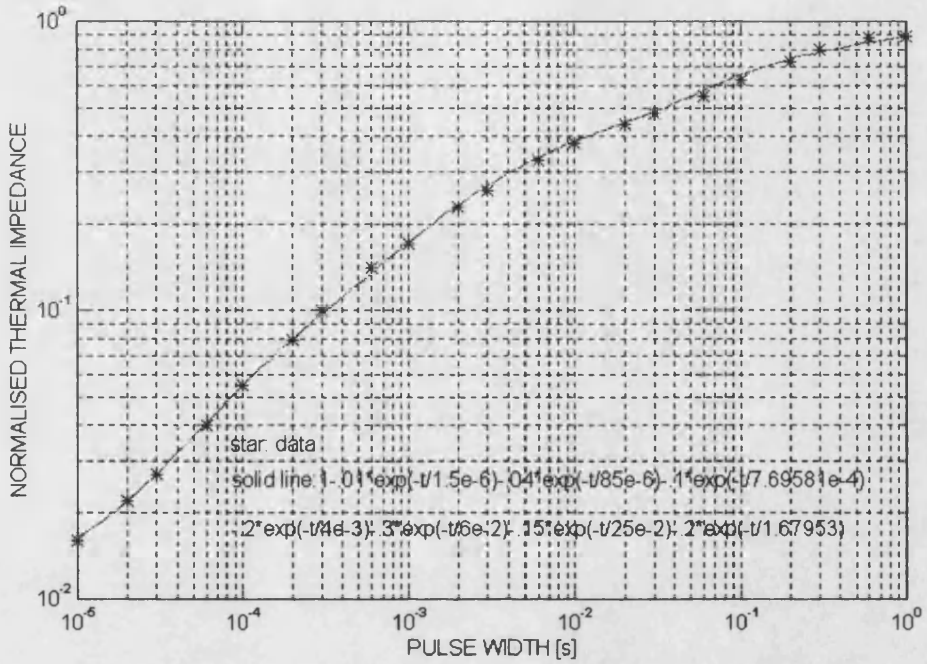
A MATLAB PROGRAM TO DRAW FIG. 14-13

```
%normalised material saving in three-limb shell-type cores
clear all
k=linspace(0,10,100);
c=0;
x1=(3*k-(.93-.406*c))./(6*(k+1));
c=.5;
x2=(3*k-(.93-.406*c))./(6*(k+1));
c=1;
x3=(3*k-(.93-.406*c))./(6*(k+1));
x4=(3*k-2)./(6*(k+1));
plot(k,x1,'r',k,x2,'b',k,x3,'g',k,x4,'--')
grid
xlabel('k')
ylabel('Normalised material saving')
gtext('c=0')
gtext('c=0.5')
gtext('c=1')
end
```

APPENDIX 14-3

```
.subckt 3_PHASE 1 2 3 4 5 6 7 8 9 10 11 12 params: LP=10 LS=1


*FIRST TRANSFORMER
K1 L11 L21 L31 1 KETD59_N67
L11 13  2 {LP}
L21  7  8 {LS}
L31 14  0 {LP}
R1 1 13 1m
E1 0 100 VALUE={V(17,4)+V(21,6)}
S1 100 101 46 0 Sabou
VS1 14 101 0
G1 2 1 VALUE={I(V1)}

*SECOND TRANSFORMER
K2  L12 L22 L32 1 KETD59_N67
L12 17  4 {LP}
L22  9 10 {LS}
L32 18 0 {LP}
S2   3 17 48 0 Sabou
V2  48 0 DC 0 AC 0 PWL 0 0 1.5u 0 1.74u .1
E3 0 102 VALUE={V(13,2)+V(21,6)}
S3 102 103 46 0 Sabou
VS3 18 103 0
V4 46 0 DC 0 AC 0 PWL 0 0 4.5U 0 5.5U .1
G2 4 3 VALUE={I(V3)}

*THIRD TRANSFORMER
K3 L13 L23 L33 1 KETD59_N67
L13 21  6 {LP}
L23 11 12 {LS}
L33 22 0 {LP}
S4   5 21 37 0 Sabou
V5 37  0 DC 0 AC 0 PWL 0 0 3.2u 0 3.5u .1
E5 0 104 VALUE={V(13,2)+V(17,4)}
S5 104 105 46 0 Sabou
VS6 22 105 0
G3 6 5 VALUE={I(V6)}

.ends 3_PHASE
```

APPENDIX 15-1



App. (15-1) Normalised thermal impedance model for MUR8100E ultra-fast-recovery diode [6]

APPENDIX 15-2

A GENERAL PROCEDURE FOR FINDING AN EQUIVALENT CIRCUIT MODEL FOR ANY THERMAL IMPEDANCE GRAPH

The normalised transient thermal impedance graph of any semiconductor device may be modelled using the following equation:

$$z_{\theta n}(t) = 1 - a_1 e^{-t/\tau_{\theta 1}} - a_2 e^{-t/\tau_{\theta 2}} - \ldots - a_n e^{-t/\tau_{\theta n}} \qquad \text{(A15-1)}$$

keeping in mind that $a_1 + a_2 + \ldots + a_n = 1$, where n is number of series-connected network branches as shown in Fig. 3-4, τ_i is the time-constant of the i^{th} branch, $\tau_i = R_{\theta i} C_{\theta i}$, a_i is the coefficient of the exponential terms, $a_i = \frac{R_{\theta i}}{R_\theta}$, and R_θ is the thermal resistance given in data sheets.

The procedure may be performed in two stages; the first is by using MATLAB to get a rough idea about the coefficients following trial-and-error method; the second is by using curve-fitting software, such as in EASYPLOT. The aim is to get a graph which matches as closely as possible the thermal impedance graph given in manufacturer's data sheets.

Stage one: MATLAB:

1. Build a data table from the data sheet relating the normalised transient thermal impedance to the pulse width taking as many points as you can. We found it convenient to take five point for each decade of the pulse-width scale at points 1, 2, 3, 6 and 8.

2. Start with the following equation to match the upper part of the thermal graph, (0.1-1) s.

$$1 - a_n e^{-t/\tau_n} \qquad \text{(A15-2)}$$

Initial values for τ_n may lie within the range (1-7)s, and for a_n within the range (0.1-0.5).

3. Plot Eq. (A15-2) and the data points of the data table, and try to match the upper part of the range (0.1-1)s by changing τ_n and a_n accordingly. The lower part of the curve, i.e. around 0.1 s, will be left slightly higher than the corresponding data points.
4. Use the following equation to match the second part of the thermal curve, (0.01-0.1)s:

$$1 - a_{n-1} e^{-t/\tau_{n-1}} - a_n e^{-t/\tau_n} \qquad \text{(A15-3)}$$

by fixing τ_n and a_n, and changing τ_{n-1} and a_{n-1}. The points around 0.1 s should be well matched and the points around 0.01 s are left slightly higher than the data points, as in step 3 above.

5. Repeat step 4 by adding more terms to Eq. (A15-3) until all data points have been matched. The number of terms, or branches, required to match the thermal impedance curve depends on the nature of the given curve.

<u>Stage two: EASYPLOT:</u>

1. Use the final equation you obtained from the first stage to fit the data points, by fixing all values you obtained except a_{n-1}, a_n, τ_{n-1} and τ_n, which is left for EASYPLOT to solve. Take note of the new values of a_{n-1}, a_n, τ_{n-1} and τ_n.
2. Fix the new values of a_n and τ_n, and leave a_{n-2}, a_{n-1}, τ_{n-2} and τ_{n-1} for EASYPLOT to solve.

3. Repeat this procedure until all terms have been fitted. You should keep in mind that $a_1 + a_2 + ... + a_n = 1$ is always achieved.

Once a_i and τ_i have been obtained, thermal resistances and capacitances of each branch may be found from the following formulae:

$$R_{\theta i} = a_i R_\theta, \; C_{\theta i} = \frac{\tau_i}{R_{\theta i}} \qquad \text{(A15-4)}$$

The sum of the individual thermal resistances should, in this case, be equal to the thermal resistance, i.e. $R_\theta = \sum_{i=1}^{i=n} R_{\theta i}$.

V_{DS} [V]	0	1.25	2.5	3.75	5	7.5	10	12.5	15	17.5	20
C_{rss} [pF]	4000	2299	1600	1179	990	735	560	465	380	330	290

V_{DS} [V]	22.5	25	27.5	30	32.5	35	37.5	40	42.5	45	50
C_{rss} [pF]	250	223	186	177	149	130	102	98	88	75	37

App. (15-3) C_{rss} variations with V_{DS} for IRFP450 [4]

V_{DS}[V]	-20	-5	-4	-3.4	-3.2	-3	-2.8	-2.6	-2.4	-2.2
C_{rss}[nF]	11	10.9	10.7	10.5	10.4	10.3	10.1	10	9.9	9.75

V_{DS}[V]	-2	-1.8	-1.6	-1.4	-1.2	-1	-0.9	-0.8	-0.7	-0.6
C_{rss}[nF]	9.6	9.5	9.4	9.3	9.1	8.9	8.7	8.5	8.2	8

V_{DS} [V]	-0.5	-0.4	-0.3	-0.2	-0.1	0	0.1	0.2	0.3	0.4
C_{rss}[nF]	7.7	7.4	7.1	6.7	6.5	6.2	5.6	5.1	4.6	4.1

V_{DS} [V]	0.5	0.6	0.7	0.8	0.9	1	1.2	1.4	1.6	1.8	2
C_{rss}[nF]	3.7	3.3	3	2.7	2.4	2.2	1.8	1.6	1.4	1.3	1.3

V_{DS} [V]	2.2	2.4	2.6	2.9	3.3	4	5	6.4	8.6	12	18.5
C_{rss}[nF]	1.2	1.2	1.1	1.1	1	0.9	0.8	0.7	0.6	0.5	0.4

V_{DS} [V]	20	50	100	200
C_{rss}[nF]	0.385	0.05	0.002	0

App. (15-4) C_{rss} variations with V_{DS} as measured by precision component analyser

```
.subckt crss 10 100
 E1 30 100 (10,100) 1
 V1 30 40 0
 R1 40 60 0.001m
 C1 60 100 1n
 H1 50 100 V1 1                    * dVGD / dt
 E2 70 100  table {V(10,100) ...}  *see App's (15-6) and (15-7) for C values
 G1 10 100 value = { V(70,100)* V(50,100) }   * i = CGD dVGD/dt
 R2 70 100 10G
 .ends
```

App. (15-5) The netlist for the sub-circuit of Fig. 15-12

V_{DS}[V]	-10	-5	-3.2	-2	-1	-0.5	0
C_{GD}[nF]	11	10.9	10.4	9.6	8.9	7.7	6.2

0.5	1	2	4	8.6	20	50	200
3.7	2.2	1.3	0.9	0.6	0.385	0.05	0

App. (15-6) C_{GD} variations with V_{DS}, as taken from measurements

V_{DS}[V]	0	1.25	2.5	3.75	5	10	15
C_{DS}[nF]	0.98	0.9	0.85	0.8	0.76	0.586	0.409

20	30	40	50	200
0.311	0.207	0.165	0.15	0.02

App. (15-7) C_{DS} variations with V_{DS}, as taken from data sheet

Frequency [Hz]	20	100	300	500	800	1k	1.5k	2k
C [nF]	9.4	9.16	8.98	8.88	8.81	8.76	8.7	8.66

Frequency [Hz]	5k	8k	10k	20k	40k	100k	200k	300k
C [nF]	8.57	8.51	8.48	8.42	8.36	8.3	8.3	8.2

(a) bias=zero

Frequency [Hz]	20	100	300	500	800	1K	1.5K	2K
C [nF]	8.9	8.57	8.42	8.35	8.3	8.2	8.17	8.15

Frequency [Hz]	5K	8K	10K	20K	40K	100K	200K	300K
C [nF]	8.07	8.03	8.01	7.97	7.91	7.86	7.8	7.7

(b) bias=20V

App. (15-8) The variations of 10 nF ceramic capacitor with frequency and bias voltage

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